Performance Productivity Challenges and Researches

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Acknowledgement: The contributions from Youfeng Wu from PSL, Intel and other members of PCL Intel

Agenda

- Performance Productivity Gap
- What Created the Gap
- Past and Current Research
- Summary

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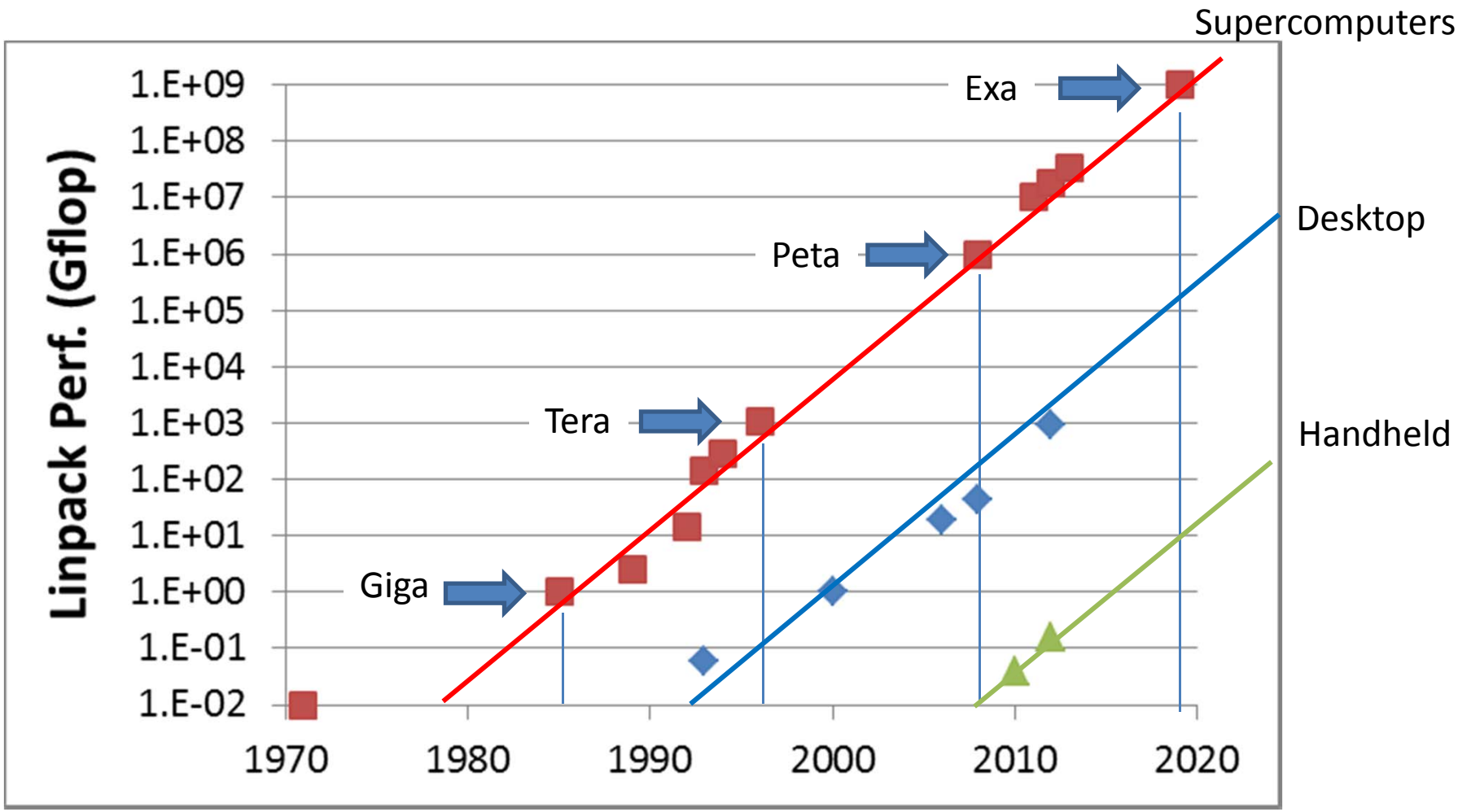
Compute Performance Roadmap



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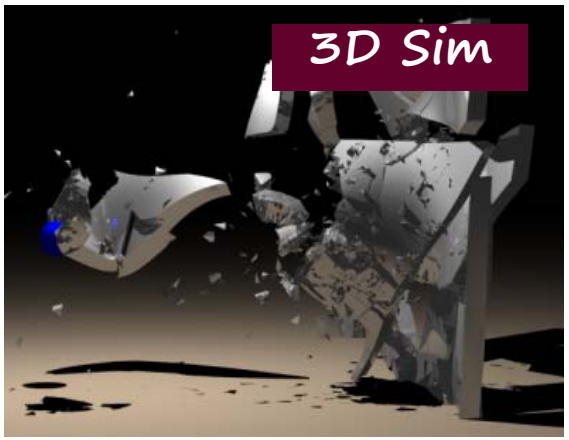
Endless Opportunities



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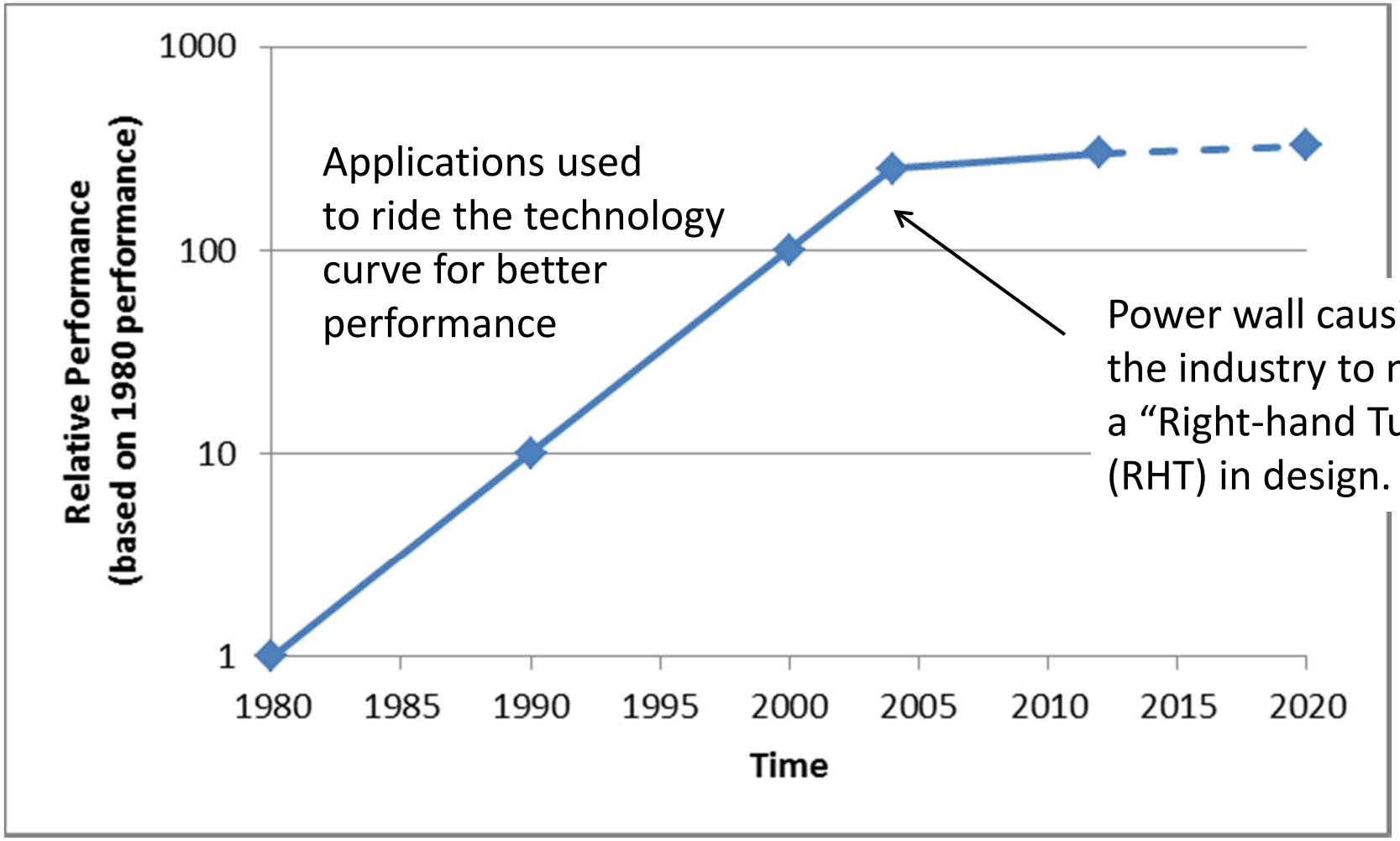
Application Performance Implications



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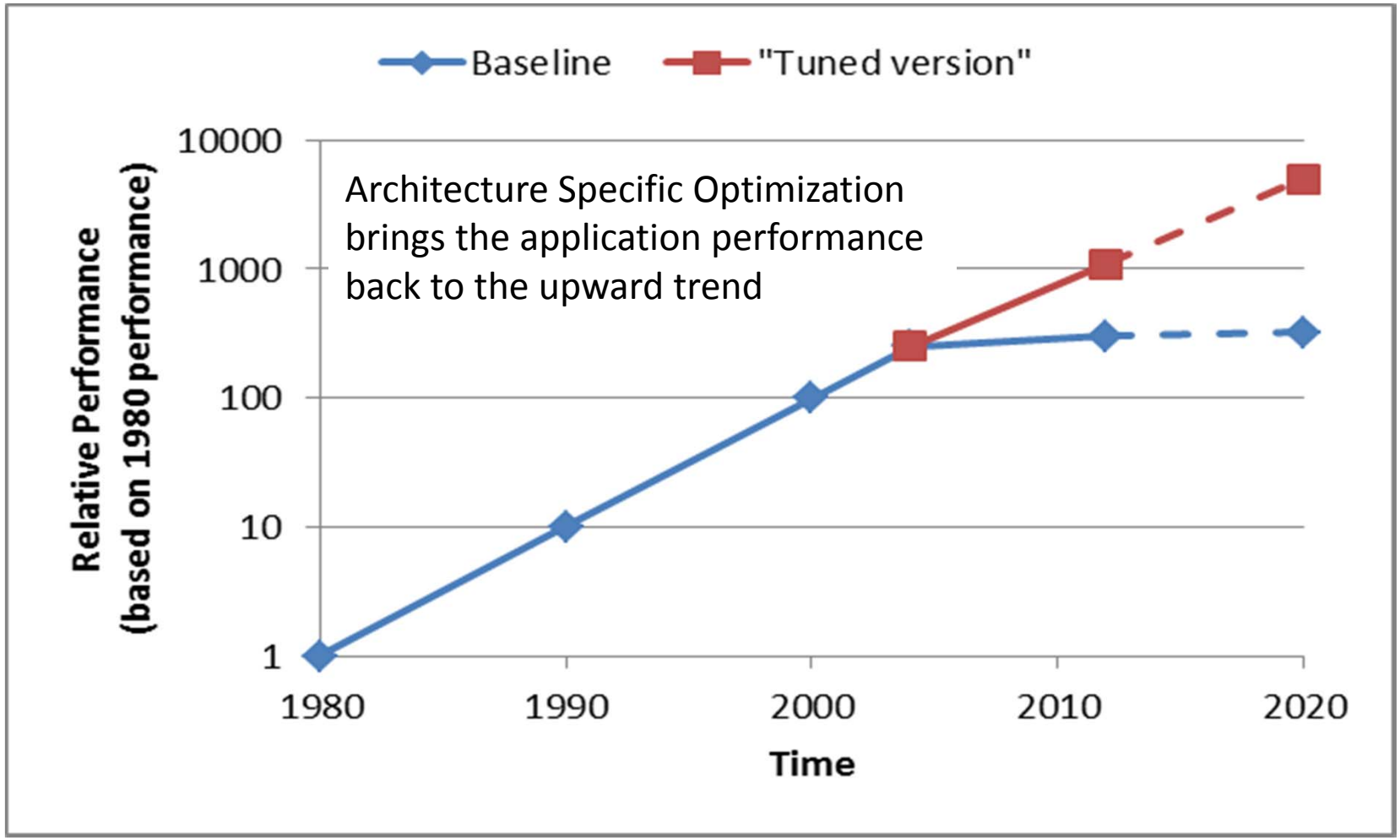
Architecture Specific Optimization



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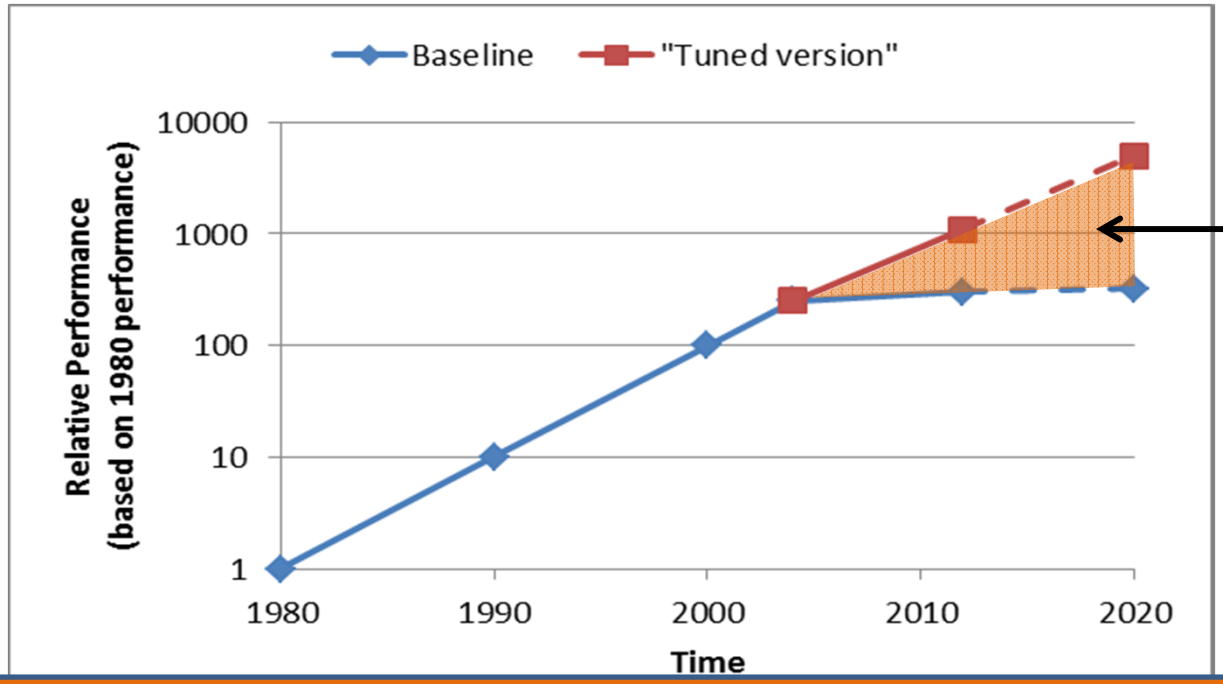
Performance Productivity Gap

- Definition: performance difference between existing software and the optimized software



"Performance-Productivity gap"

"Performance Productivity Gap" = Opportunity Lost

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Mini-Summary 1

- Moore's law is alive and well. Future processors to have many cores and great performance potential
- Current SW experience "Performance Productivity Gap" and can lead to competitive disadvantages

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- Past and Current Research
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Sources of Performance Productivity Gap

- The obvious:
  - Many cores
  - The memory

- The not so obvious:
  - Energy efficiency challenge
  - Heterogeneity
  - Core variations
  - Failures

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Problem w/ Parallel Computing

- Parallel systems
  - In the past, are for the HPC programmers
  - Result of the industry “RHT”, parallel systems are for everyone now
- Why parallel computing is hard
  - People tends to think sequentially
  - Very few are taught to write parallel programs
  - Simply extending serial programs will not get good performance and will be hard to debug

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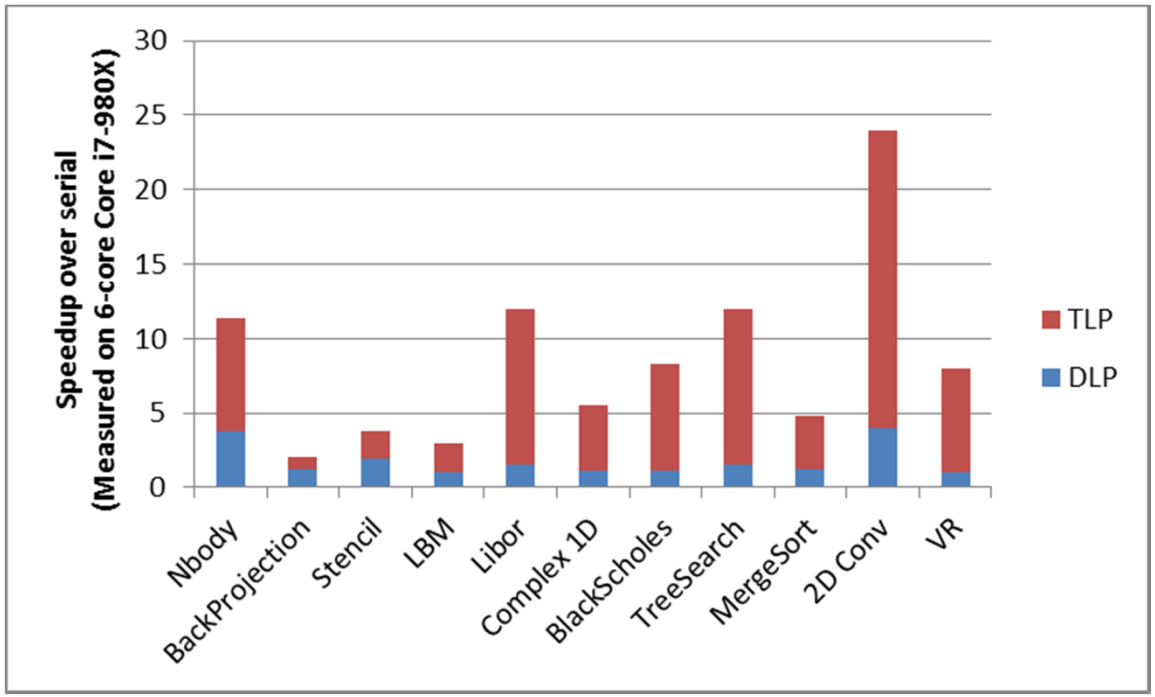
Parallel Opportunity / Challenges

Exploring multi-core and SIMD can result in significant speedup



* Data drawn from Satish et. al. "Can Traditional Programming Bridge the Ninja Performance Gap for Parallel Computing Applications?", In proc. of ISCA 2012

Thread Level Parallelism (TLP) Challenges:

- Think concurrency
- Data/task decomposition
- Synchronization

Data Level Parallelism (DLP) Challenges:

- Data alignment
- Control flow divergence

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Problem in Feeding

- Feeding one core is hard enough
  - Memory performance lags processor performance
    - Survey shows: Processor improves 50% a year, memory BW improves ~20%, and memory latency improves ~5% a year

- Feeding many cores is much harder
  - Not enough BW to go around
  - Conflicts and contention

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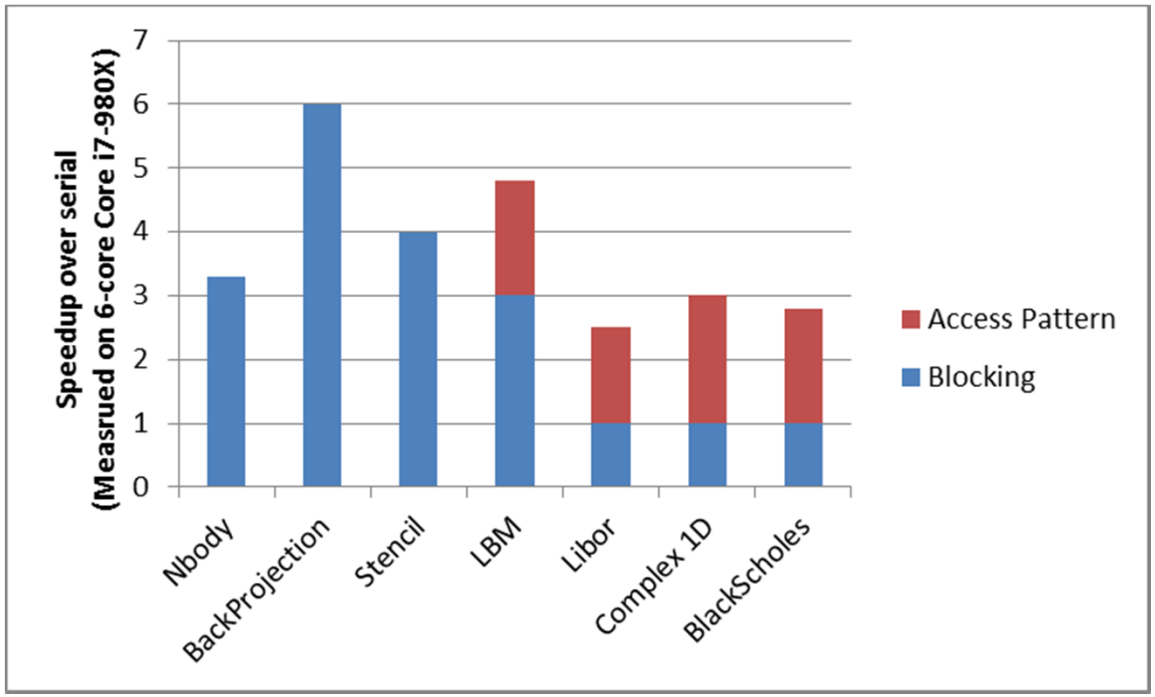
Data Access Opportunity / Challenges

Optimizing data access patterns and making use of cache / local memory can mitigate data access problem



* Data drawn from Satish et. al. "Can Traditional Programming Bridge the Ninja Performance Gap for Parallel Computing Applications?", In proc. of ISCA 2012

Challenges:

- No standardize memory hierarchy
- Intuitive data structure is not necessary optimal for modern memory subsystem

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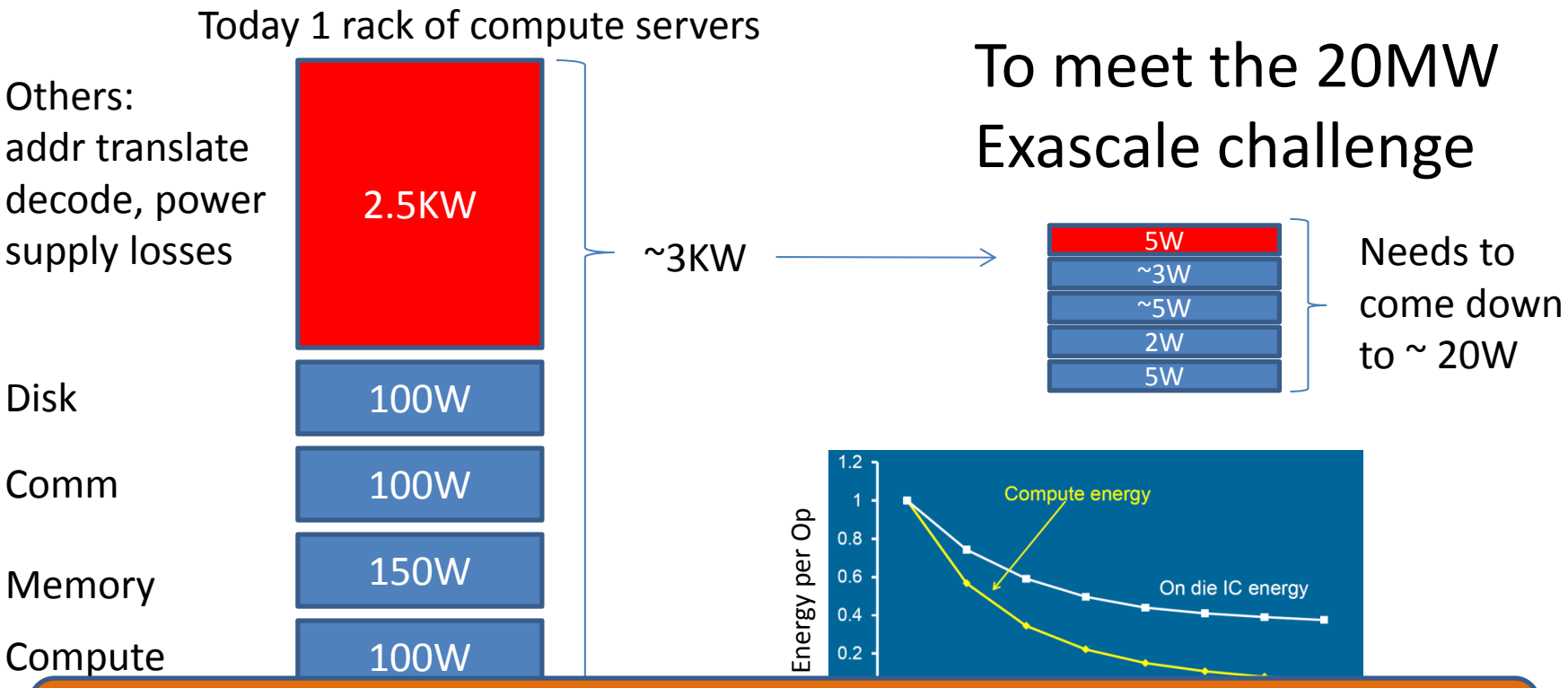
THE NOT SO OBVIOUS CAUSES

Energy Efficiency Challenge

- Today 50PF computer at 30MW power



More efficient application can help energy issue

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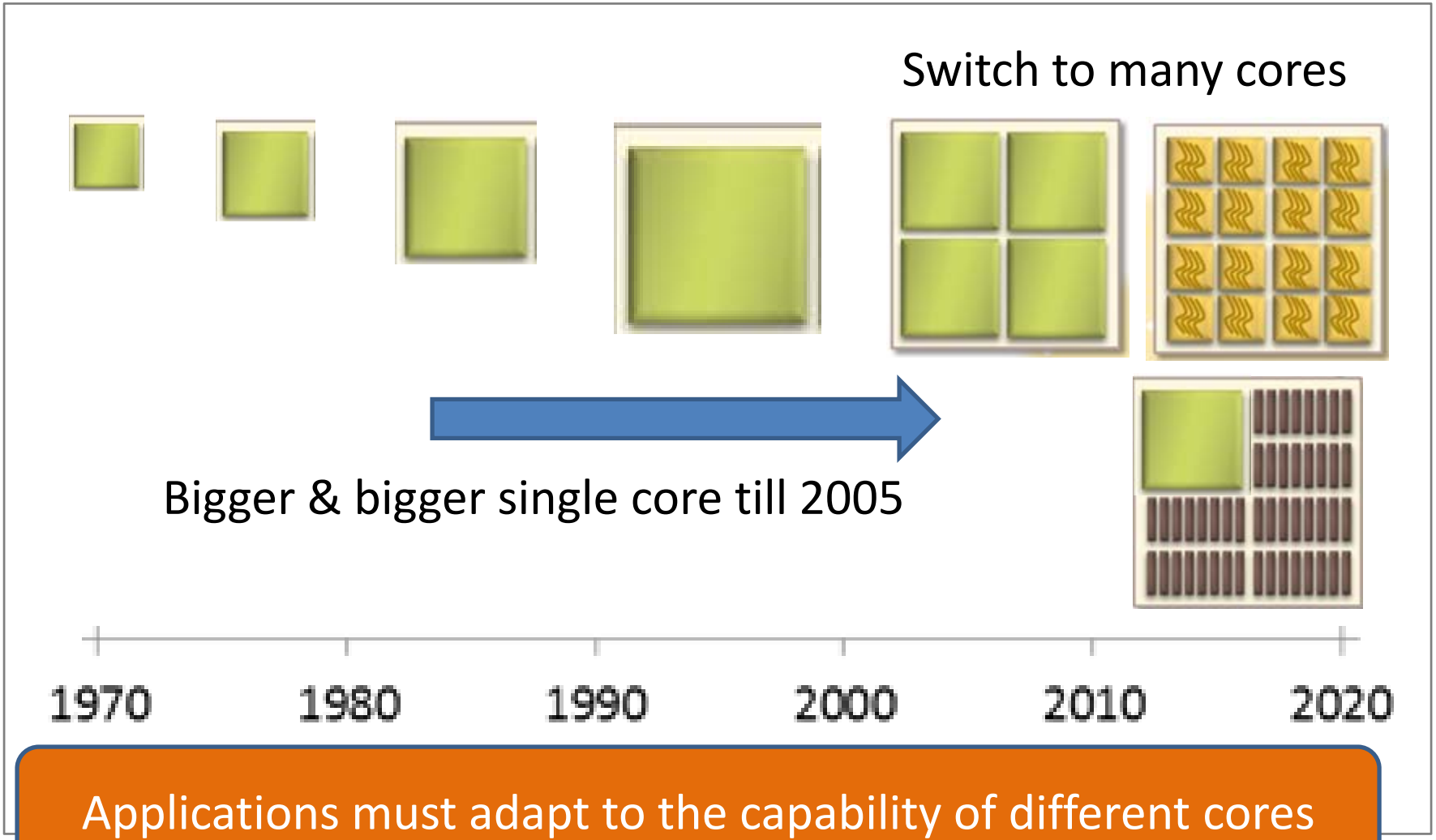
Heterogeneity is Here



Applications must adapt to the capability of different cores

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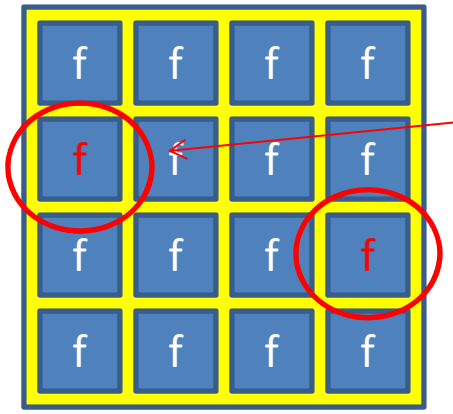
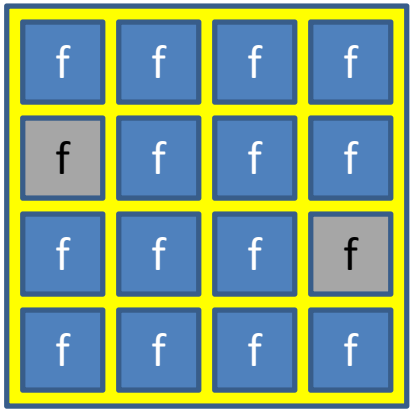
Manufacturing Variations

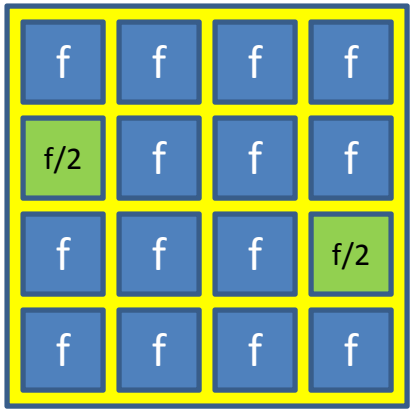


Some cores will inherently runs slower

Soln1: Turn them off



Soln2: Turn them @ diff freq



Again application must adapt to core variation

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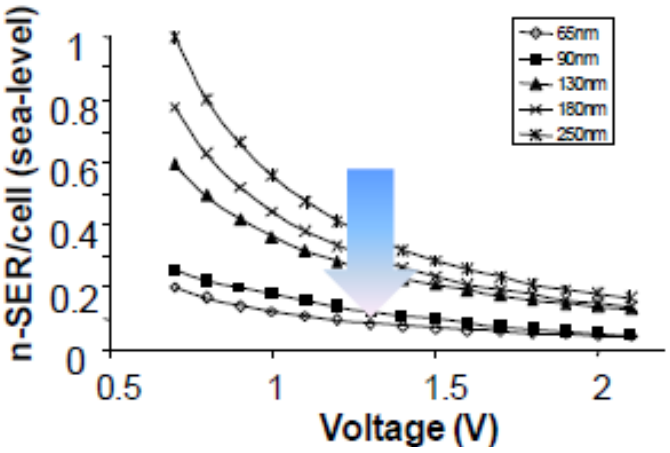
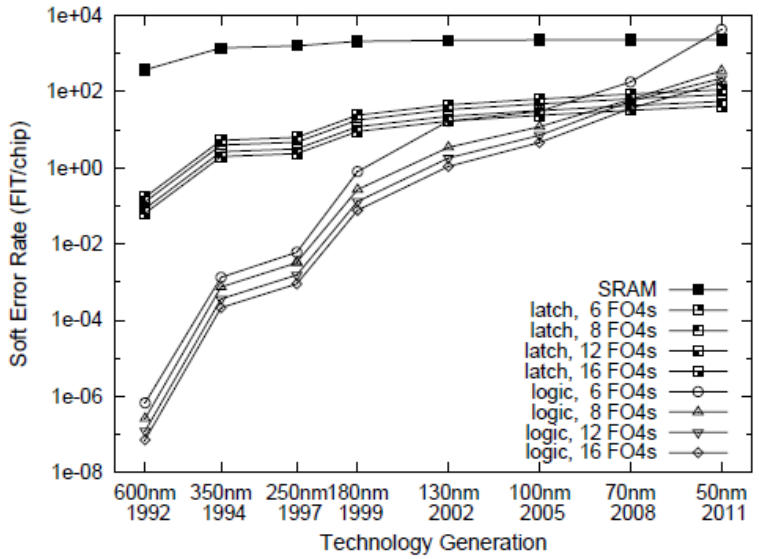
Tolerating Faults

- Smaller feature sizes reduce soft error rate
- Increases in # of components per chip cause overall error rate to increase





Premkishore Shivakumar, et al. *Modeling the Impact of Device and Pipeline Scaling on the Soft Error Rate of Processor Elements*. Computer Science Department, University of Texas at Austin, 2002.

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Mini-Summary 2

- An array of technology challenges cause the performance productivity gap
- Significant performance opportunity but lots of challenges

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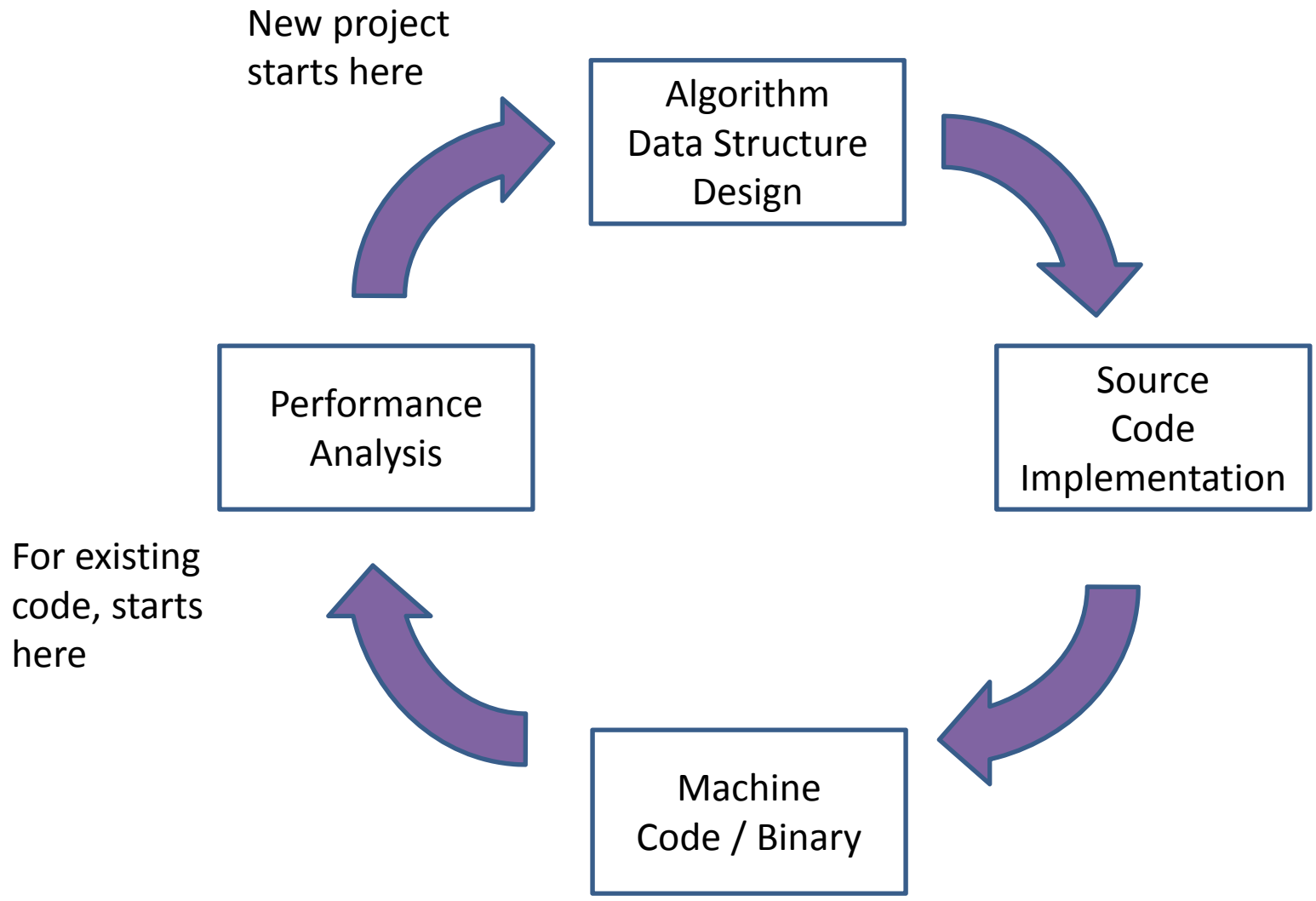
Program Development Workflow



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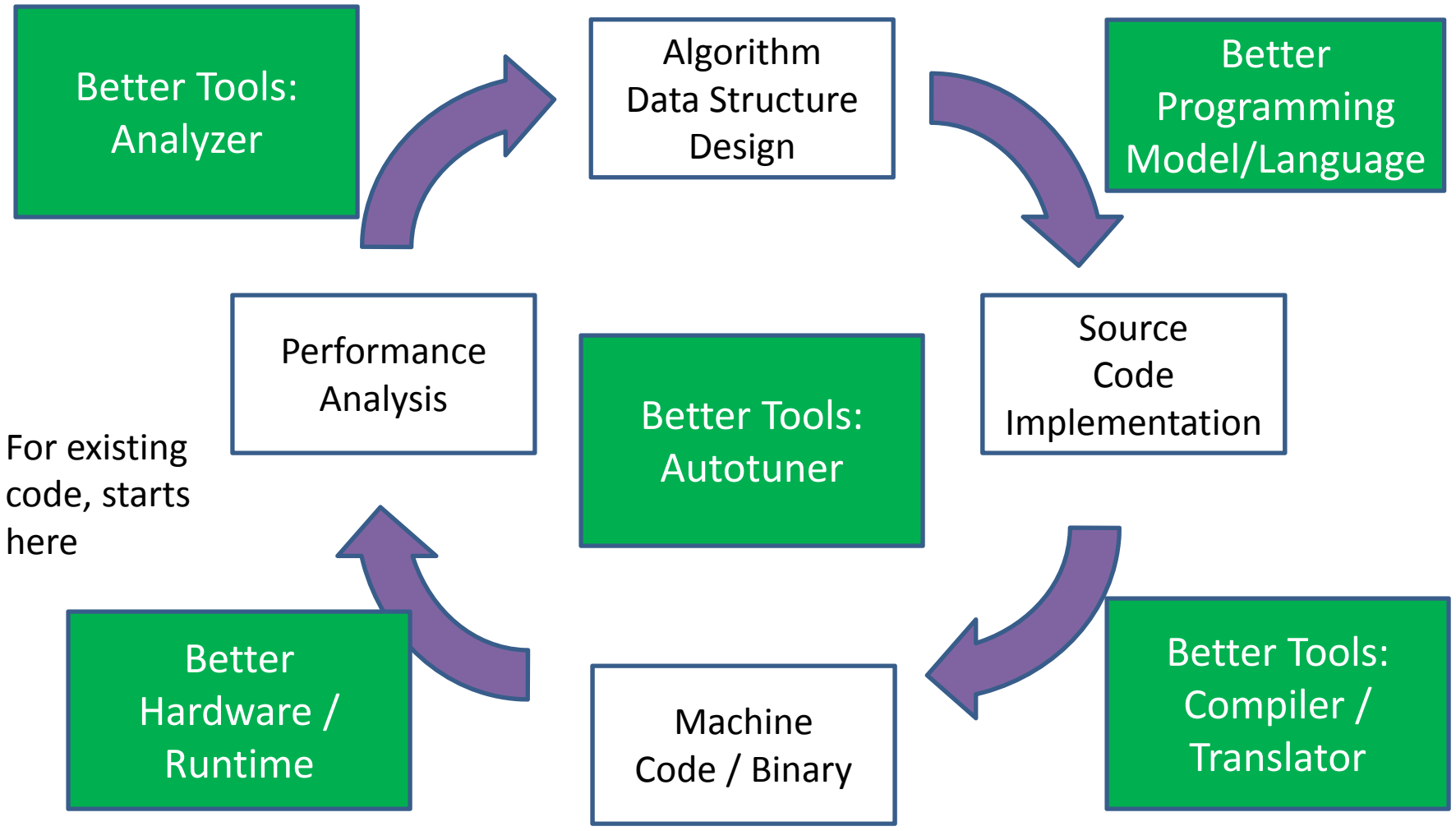
Opportunities to Bridge the Performance Productivity Gap



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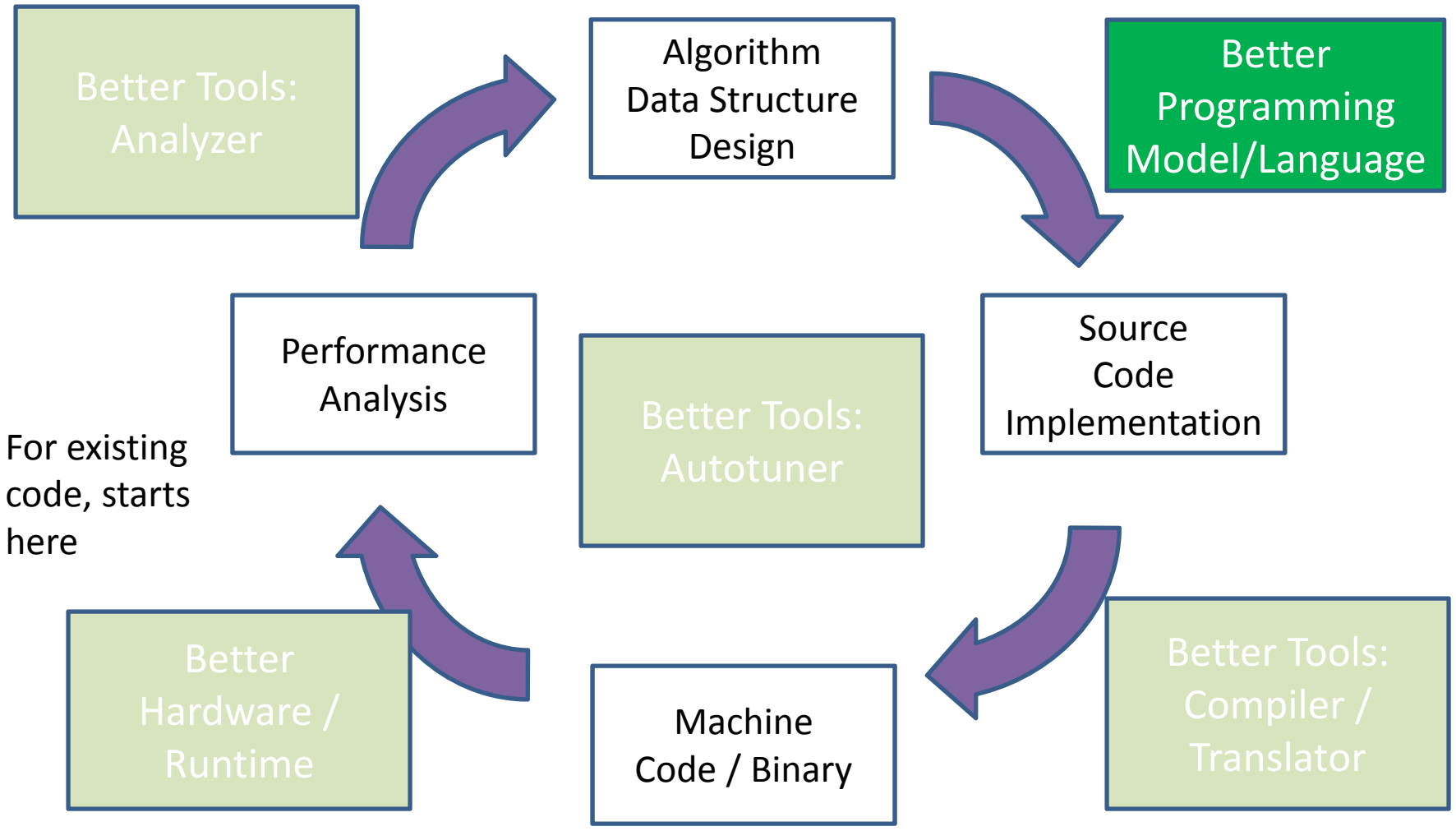
Programming Model Language & Perf-Productivity Gap



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Desired Properties

- Allow programmers to:
  - Express concurrency (at different levels)
  - Manage data locality
  - Provide determinism to aid debug
- Other goodies:
  - Portability across architecture
  - Easy code reuse
  - Distributed development

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Approaches

- Library extensions of existing sequential languages
  - E.g., SHMEM, MPI, PVM
- Directives based
  - OpenMP, OpenACC
- New parallel languages
  - Charm++, CILK, Co-Array Fortran, Titanium, UPC, X10, Fortress, Chapel, CUDA, OpenCL, Parallel JavaScript

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Chapel, Fortress and X10

	Chapel	Fortress	X10
Parallel model	Concurrent Tasks	Parallel Tasks	Concurrent Activities
Array Data Types / Pointers	Yes	Yes	Yes
Data management	PGAS w/ Locale	PGAS on arrays	PGAS w/ Place

```
config var n = 5,                       // size of n x n grid
           epsilon = 0.00001;           // convergence tolerance

def main() {
  const ProblemSpace = [1..n, 1..n],    // domain for grid points
        BigDomain = [0..n+1, 0..n+1];   // domain including boundary points

  var X, XNew: [BigDomain] real = 0.0;  // declare arrays:
                                        //   X stores approximate solution
                                        //   XNew stores the next solution

  X[n+1, 1..n] = 1.0;                   // Set south boundary values to 1.0

  var iteration = 0,                    // iteration counter
      delta: real;                      // measure of convergence

  const north = (-1,0), south = (1,0), east = (0,1), west = (0,-1);

  do {
    // compute next approximation using Jacobi method and store in XNew
    forall ij in ProblemSpace do
      XNew(ij) = (X(ij+north) + X(ij+south) + X(ij+east) + X(ij+west)) / 4.0;

    // compute difference between next and current approximations
    delta = max reduce abs(XNew[ProblemSpace] - X[ProblemSpace]);

    // update X with next approximation
    X[ProblemSpace] = XNew[ProblemSpace];

    // advance iteration counter
    iteration += 1;

  } while (delta > epsilon);

}
```

```
component fortress.executable

export Executable

run(args:String...):()=do

   needleLength = 20                          // declaration of
   numRows = 10                               // immutable variables
   tableHeight = needleLength numRows

   var hits : RR64 = 0.0                      // declaration of mutal
   var n : RR64 = 0.0                         // variables of type RI

   for i <- 1#3000 do                         // 3000 iterations
      delta_X = random(2.0) - 1
      delta_Y = random(2.0) - 1
      rsq = delta_X^2 + delta_Y^2

      if 0 < rsq < 1 then
         y1 = tableHeight random(1.0)
         y2 = y1 + needleLength (delta_Y / sqrt(rsq))
         (y_L, y_H) = (y1 MIN y2, y1 MAX y2)

         // increase 'hits' if needle hits line
         if ceiling(y_L/needleLength) = floor(y_H/needleLength) then
            atomic do hits += 1.0 end
         end
         atomic do n += 1.0 end
      end
   end

   probability = hits/n
   pi_est = 2.0/probability
   end
end
```

```
public class Jacobi extends x10Test {

    const int N = 5;                            // size of grid
    const double epsilon = 0.0001;              // convergence tolerance
    const double epsilon2 = 0.000000001;

    const region(:rank==2) RInner = [1:N, 1:N]; // region for grid points
    const region(:rank==2) R = [0:N+1, 0:N+1];  // region including boundary
                                                // points

    // distribution of grid
    const dist(:rank==2) D = (dist(:rank==2)) dist.factory.block(R);
    const dist(:rank==2) DInner = D | RInner;    // distribution for inner region of grid
    const dist(:rank==2) DBoundary = D - RInner; // boundary region of grid

    const int EXPECTED_ITERS = 97;
    const double EXPECTED_ERR = 0.0018673382039402497;

    final double[.] XNew = new double[D] (point p[i,j]){
        return DBoundary.contains(p) ? (N-1)/2 : N*(i-1)+(j-1);
    };

    public boolean run() {
        int iters = 0;
        double err;
        while (true) {
            final double[:distribution==this.DInner] X = new double[DInner] (point [i,j]){
                return (XNew[i+1,j]+XNew[i-1,j]+XNew[i,j+1]+XNew[i,j-1])/4.0;
            };
            if ((err = ((XNew | this.DInner)-X).abs().sum()) < epsilon) break;
            XNew.update(X);
            iters++;
        }
        System.out.println("Error = "+err);
        System.out.println("Iterations = "+iters);
        return Math.abs(err-EXPECTED_ERR) < epsilon2 && iters == EXPECTED_ITERS;
    }

    public static void main(String[] args) {
        new Jacobi().execute();
    }
}
```

Codes extracted from Michele Weiland, "Chapel, Fortress and X10: Novel languages for HPC", *The University of Edinburgh, Tech. Rep., October* (2007).

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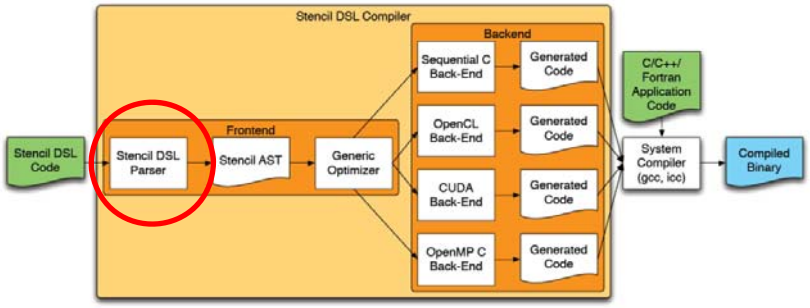
Domain Specific Languages

DSLs trade off generality to better enable back-end tools performance and portability

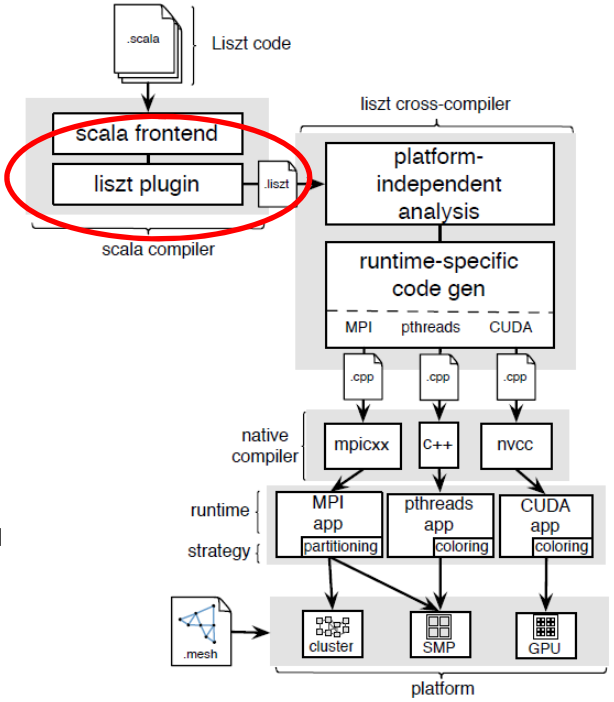
- Stencil DSL [Holewinski'12]

  Write stencil as point function and grid rather than loop-nest



Stencil Compiler Workflow

- Liszt [DeVito'11] : for mesh -based PDE solver



[Holewinski'12] Justin Holewinski, et al. "High-performance code generation for stencil computations on GPU architectures."*Proceedings of the 26th ACM international conference on Supercomputing*. ACM, 2012.

[DeVito'11] Zachary DeVito, et al. "Liszt: a domain specific language for building portable mesh-based PDE solvers." *Proceedings of 2011 International Conference for High Performance Computing, Networking, Storage and Analysis*. ACM, 2011.

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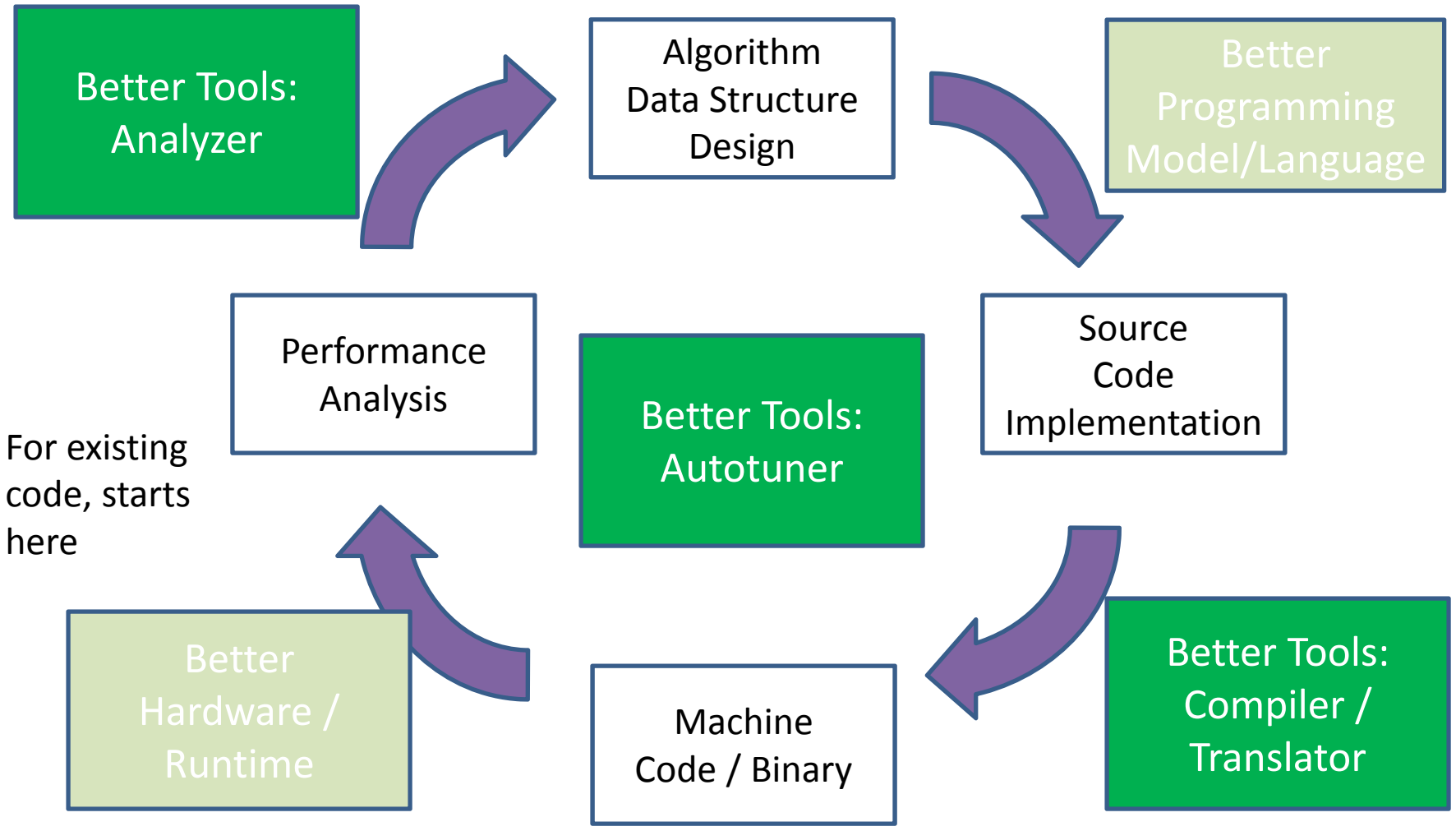
Tools & Perf-Productivity Gap



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Tools

Tools help manage the low level implementation details for parallelism & data management

- Compiler
- Analyzer
- Auto-tuner

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Compiler Optimizations

- Parallelization (and vectorization)
  - Focus on picking out independent tasks to form threads of execution through data/control dependency analysis
    - E.g., Independent loop iterations can be parallelized as different threads
  - More recent work:
    - Speculative parallelization – requires special HW support
    - Semi-automatic parallelization – requires programmers to help annotate the section that can be parallelized
  - Some reference: SUIF, Polaris, Helix, DSWP, Cray compiler, Intel C++ Compiler

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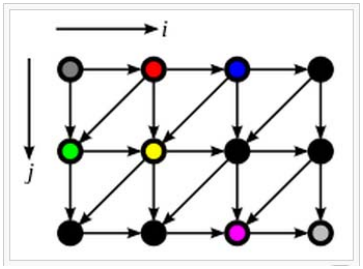
Compiler Optimizations

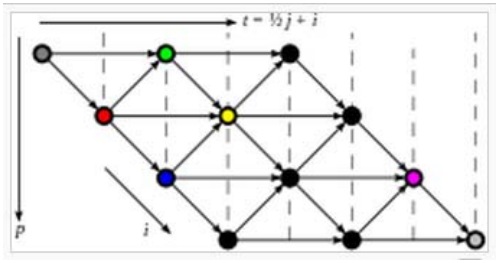
- Array padding and tiling
  - Padding to minimize access conflicts
  - Use static analysis to identify the optimal blocking factor to maximize reuse
  - Complications include: multiple level tiling, alignment, data placement, load balance

- Loop transformation:
  - Reshape the execution within a loop to improve program execution as well as data locality
  - State-of-the-art uses polyhedral models to handle a wider class of programs



j first, followed by i

A[i][j] <- A[i-1][j], A[i][j-1] and A[i+1][j-1]



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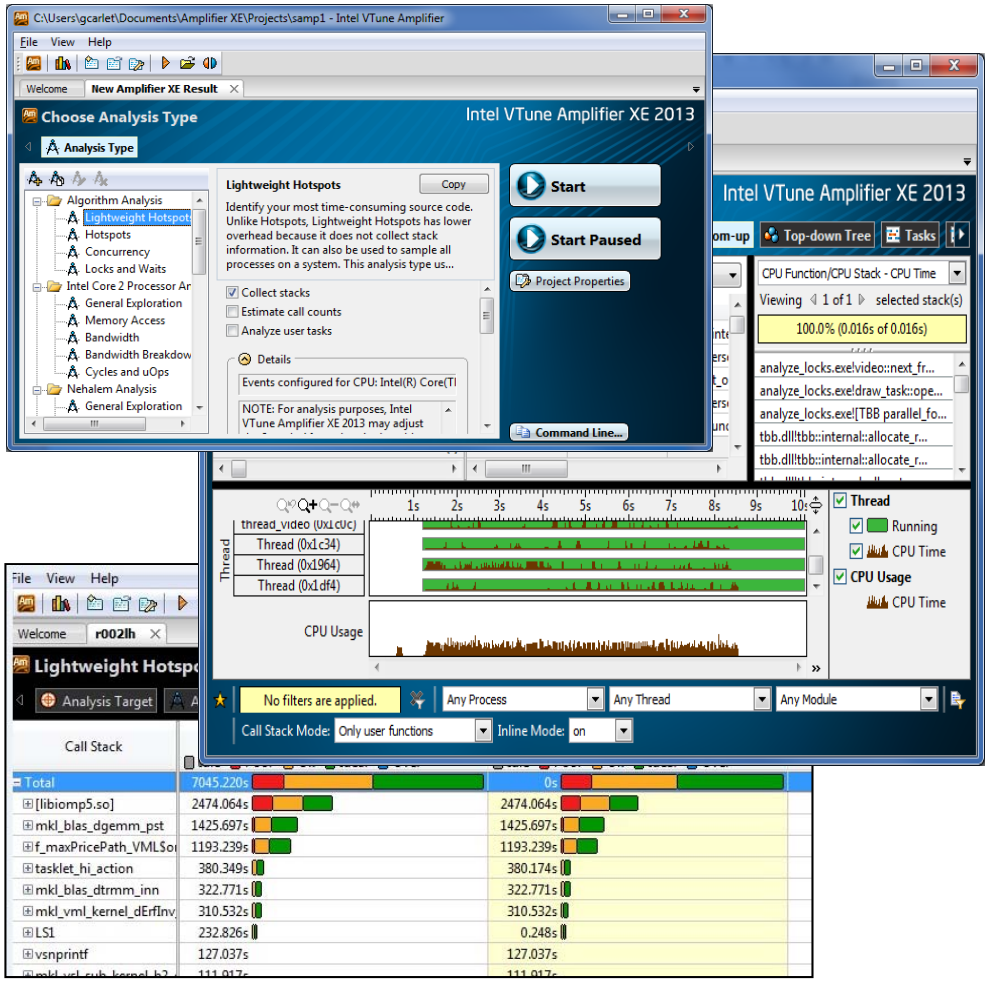
Performance Analyzer(s)

- Performance Analyzer:
  - Papi
  - Perf
  - Likwid
  - Gprof
  - Valgrind/kCacheGrind
  - IBM Tivoli

- Other IDEs:
  - Eclipse
  - Microsoft® Visual Studio
  - Xcode from Apple®

- Intel® VTune™ Performance Analyzer



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Auto-tuner

- Use machine time in place of human time for tuning
- Basic technique is to search over possible implementation
- Recent work start to explore statistical machine learning method to prune search space

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Auto-tuner Examples

Search of a design space (e.g Kamil'10)

- Start w/ Fortran Spec
- Translate to IR
- Explore design space

Category	Optimization Parameter	Name	Parameter Tuning Range by Architecture Barcelona/Nehalem	Victoria Falls	GTX280
Data Allocation	NUMA Aware		✓	✓	N/A
Domain Decomposition	Core Block Size	*CX*	NX	{8...NX}	{16†..NX}
		CY	{8...NY}	{8...NY}	{16†..NY}
		CZ	{128...NZ}	{128...NZ}	{16†..NZ}
	Thread Block Size	*TX*	CX	CX	$\{1..\frac{CX}{16}\}^{\ddagger}$
		TY	CY	CY	$\{\frac{CY}{16}..CY\}^{\ddagger}$
		TZ	CZ	CZ	$\{\frac{CZ}{16}..CZ\}^{\ddagger}$
	Chunk Size		$\{1...\frac{NX \times NY \times NZ}{CX \times CY \times CZ \times NThreads}\}$		N/A
Low Level	Array Indexing		✓	✓	✓
	Register Block Size	*RX*	{1...8}	{1...8}	1
		RY	{1...2}	{1...2}	1*
		RZ	{1...2}	{1...2}	1*

Other auto-tuners: Examples: ATLAS [Whaley'01], OSKI [Vuduc'05], FLAME [Gunnels '01], FFTW [Frigo'99], SPIRAL [Puschel'05], Stencil Autotuner [Kamil'10] [Datta'08] [Ganapathi'09]

Statistical Machine Learning Model [Ganapathi'09]

- Use Kernel Canonical Correlation Analysis
- Performance within 1% of experts programmers

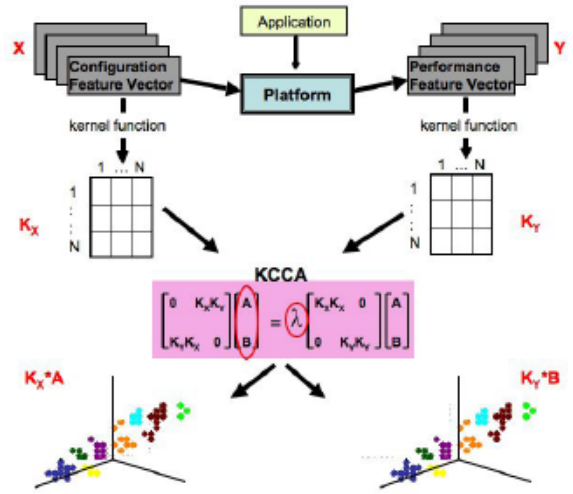

Figure 1: The KCCA methodology discovers relationships between configurations and performance.

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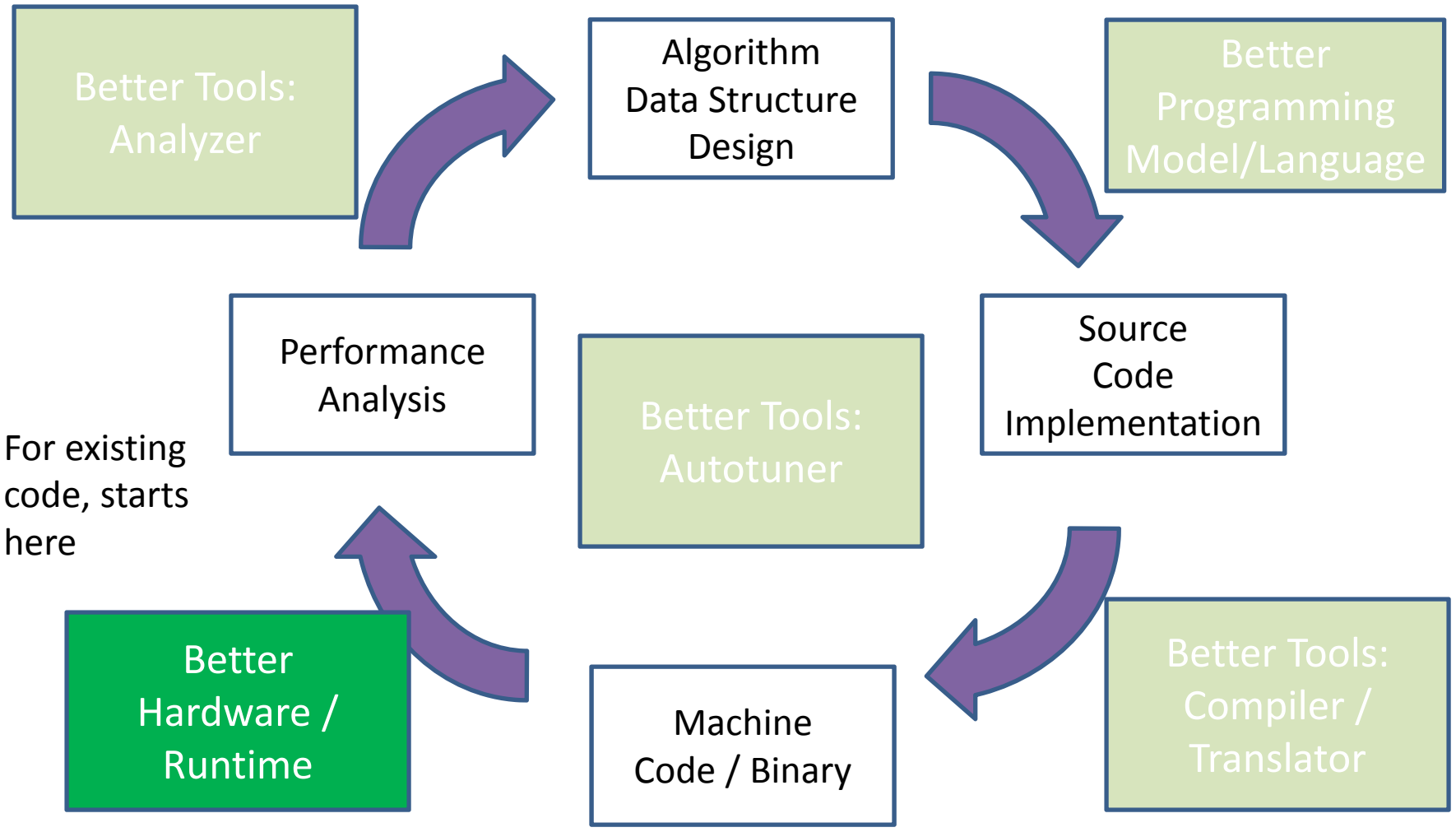
Hardware / Runtime & Perf-Productivity Gap



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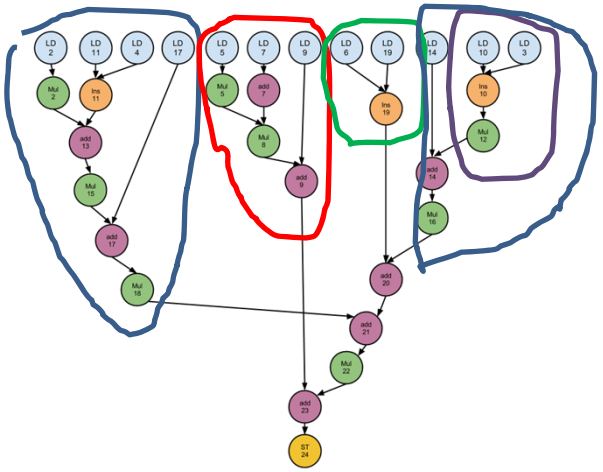
Architecture Supports for Parallelism

- Speculative parallelism
  - Allow multiple iterations or basic blocks on multiple hardware cores/units
  - Examples:
    - Multiscalar [Sohi'95] (parallelize loop iterations)
    - Decouple SW pipeline [Ottoni'05] (parallelize blocks within an iteration)
    - Cluster architecture [Marcuello'99] (group dependent instructions in the same cluster)



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Architecture Supports for Parallelism

- Managing parallelism
  - Coherent Cache
  - Dynamic load balancing
  - Fast synchronization via. full/empty bit
  - Reduction hardware
  - Transaction memory

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Architecture Supports for Data Accesses

- Tolerate the latency
  - Multi-threading
- Bring data in earlier (to hide memory latency)
  - Data prefetching
    - Hardware prefetcher, software prefetching
  - Decoupled architecture
    - Helper threads
  - Speculation
    - Value prediction (address prediction [Gonzalez'97])
    - Large Instruction window

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Architecture Supports for Data Accesses

- Conserve the available bandwidth
  - Relax consistency model
    - Allow more overlap between memory requests
  - Write buffers
    - Write buffers or Streaming stores to eliminate unnecessary BW
- Other more extreme idea:
  - Compute in Memory (e.g., IRAM)

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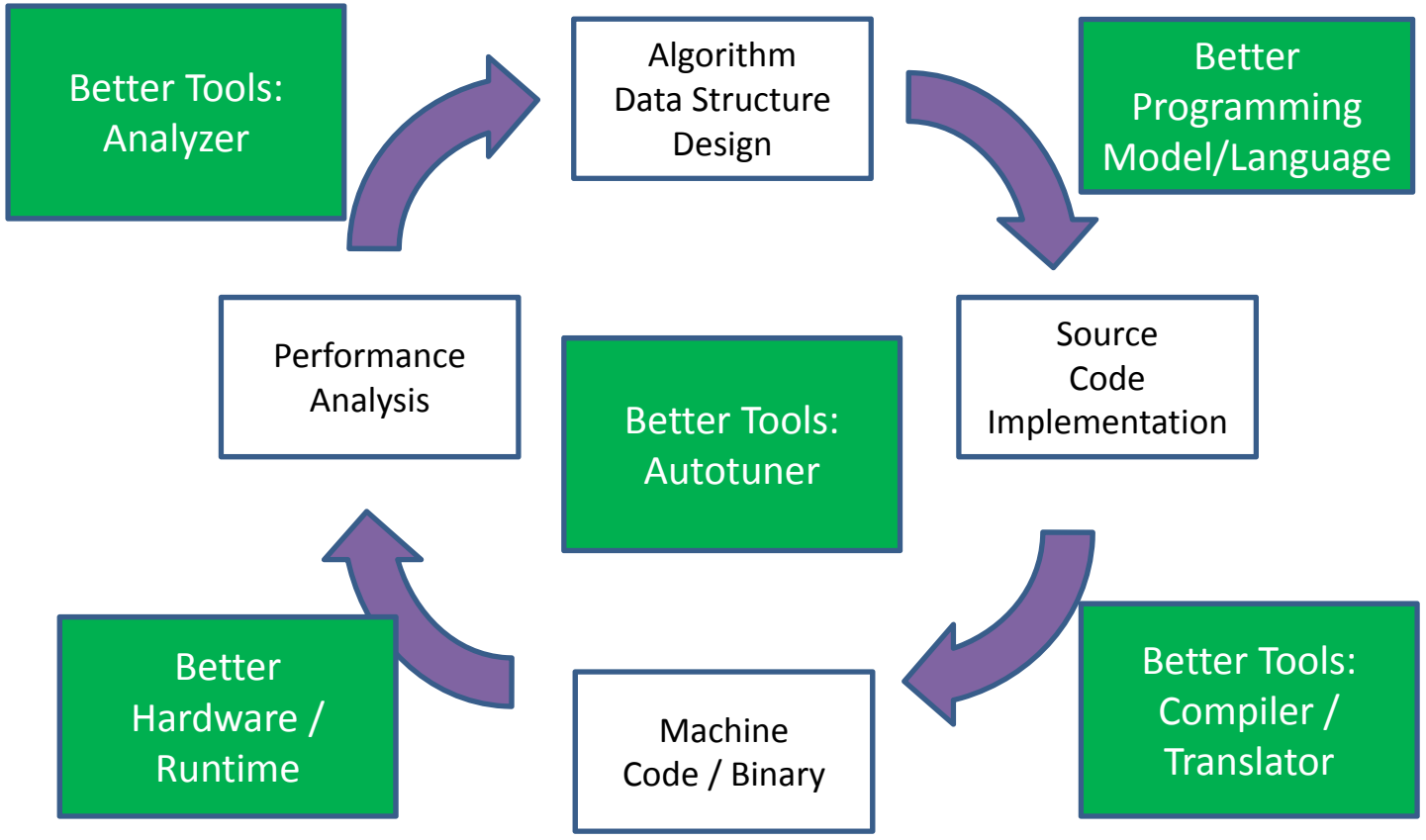
Mini-Summary 3

- A lot of great researches to build on



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Summary

- "Performance Productivity Gap" arises due to a series of technology advances and it leads to competitive disadvantages
- Integrated researches on programming model, language, tools and hardware are need to bridge the "Performance Productivity Gap"
- Many great researches, but more is needed
  - Especially in areas like heterogeneity, energy efficiency, fault tolerance, etc.

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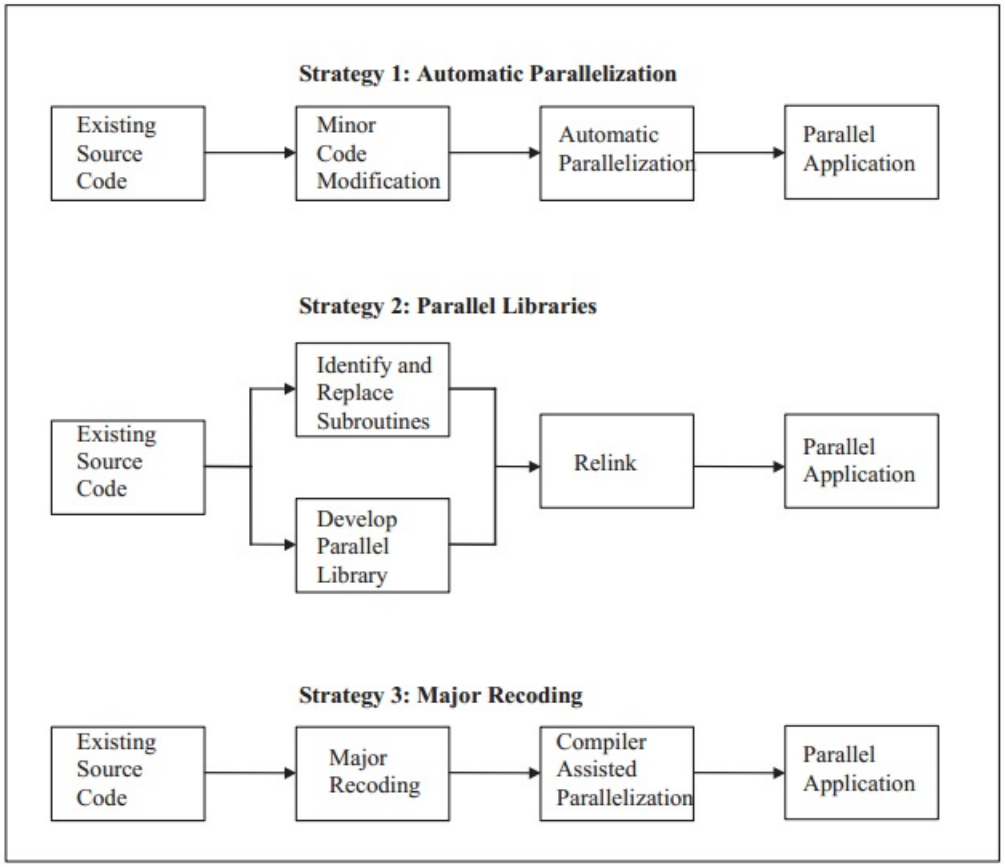
Parallelization Strategies



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