Centre de Calcul ROMEO
MAISON DE LA SIMULATION de Champagne-Ardenne

PRACE

29th VI-HPS Tuning Workshop

ROMEO, Reims, 15-19 October 2018

http://www.vi-hps.org/training/tws/tw29.html

Judit Giménez & Lau Mercadal
Barcelona Supercomputing Centre

Sameer Shende
University of Oregon

Cédric Valensi, Emmanuel Oseret, Pablo de Oliveira, Eric Petit & Yohan Chatelain
UVSQ

Fabrice Dupros
ARM

Johannes Ziegenbalg
TU Dresden

Marc Schlütter
Jülich Supercomputing Centre

Agenda (Monday)

Time	Topic	Presenter
09:00	Welcome	
	Introduction to VI-HPS & overview of tools	Shende
	Introduction to parallel performance engineering	Schlütter
	Introduction to lab setup	ROMEO
	Building and running NPB-MZ-MPI	Schlütter
10:30	*Break*	
11:00	MAQAO performance analysis tools	Oseret, Valensi
12:30	*Lunch*	
14:00	Hands-on coaching to apply tools to analyze your own code(s)	all
17:30	Review of day and schedule for remainder of workshop	
18:00	*Adjourn*	

Agenda (Tuesday)

Time	Topic	Presenter
09:00	FORGE (MAP) & performance reports	Dupros
	ARM hands-on exercises	
10:30	*Break*	
11:00	TAU performance system	Shende
	TAU hands-on exercises	
12:30	*Lunch*	
14:00	Hands-on coaching to apply tools to analyze your own code(s)	all
17:30	Review of day and schedule for remainder of workshop	
18:00	*Adjourn*	

Agenda (Wednesday)

Time	Topic	Presenter
09:00	Instrumentation & measurement with Score-P	Ziegenbalg
	Score-P hands-on exercises	
	CUBE profile explorer hands-on exercises	Schlütter
	Score-P analysis scoring & measurement filtering	
	Measuring hardware counters and other metrics	
10:30	*Break*	
11:00	Scalasca automated trace analysis, hands-on exercises	Schlütter
12:30	*Lunch*	
14:00	Hands-on coaching to apply tools to analyze your own code(s)	all
17:30	Review of day and schedule for remainder of workshop	
18:00	*Adjourn*	

Agenda (Thursday)

Time	Topic	Presenter
09:00	Vampir interactive trace analysis	Ziegenbalg
	Vampir hands-on exercises	
10:30	*Break*	
11:00	Paraver tracing tools suite	Gimenez, Mercadal
	Paraver hands-on exercises	
12:30	*Lunch*	
14:00	Hands-on coaching to apply tools to analyze your own code(s)	all
17:30	Review of day and schedule for remainder of workshop	
18:00	*Adjourn*	

Agenda (Friday)

Time	Topic	Presenter
09:00	VTune toolset	Intel
10:30	*Break*	
11:00	Verificarlo numerical accuracy analysis	Oliveira, Petit, Chatelain
	Review	
12:30	*Lunch*	
14:00	Hands-on coaching to apply tools to analyze your own code(s)	all
17:00	*Adjourn*	

Virtual Institute – High Productivity Supercomputing

- **Goal**: Improve the quality and accelerate the development process of complex simulation codes running on highly-parallel computer systems
- Start-up funding (2006–2011)
  by Helmholtz Association of German Research Centres
- Activities
  - Development and integration of HPC programming tools
    - Correctness checking & performance analysis
  - Academic workshops
  - Training workshops
  - Service
    - Support email lists
    - Application engagement

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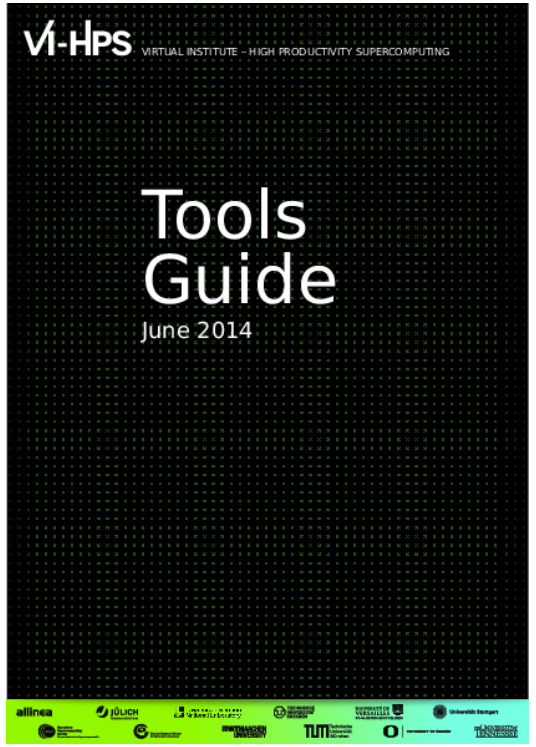
http://www.vi-hps.org

Productivity tools

- MUST & Archer
  - MPI & OpenMP usage correctness checking
- PAPI
  - Interfacing to hardware performance counters
- Periscope Tuning Framework
  - Automatic analysis and Tuning
- **Scalasca**
  - Large-scale parallel performance analysis
- **TAU**
  - Integrated parallel performance system
- **Vampir**
  - Interactive graphical trace visualization & analysis
- **Score-P**
  - Community-developed instrumentation & measurement infrastructure

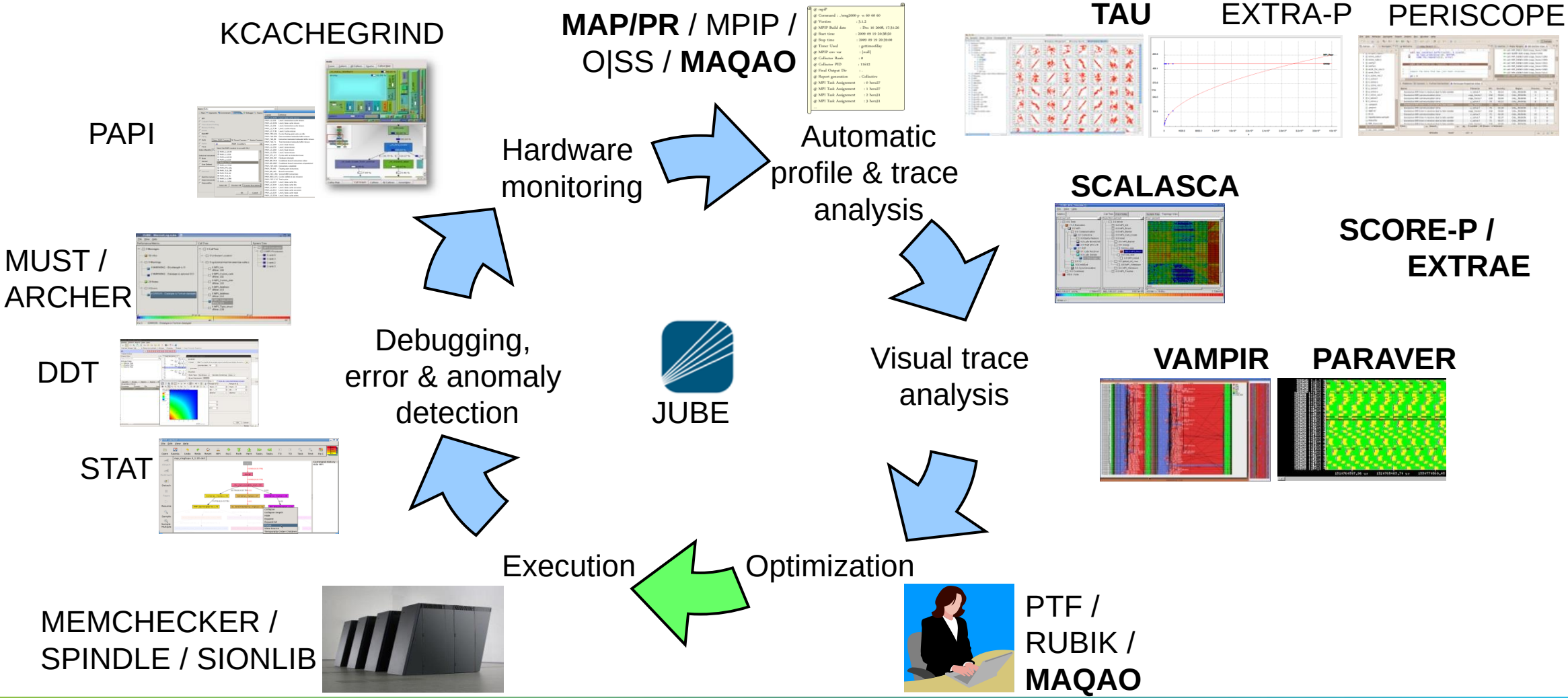
For a brief overview of tools consult the VI-HPS Tools Guide:



Productivity tools (cont.)

- DDT/**MAP/PR**: Parallel debugging, profiling & performance reports
- Extra-P: Automated performance modelling
- Kcachegrind: Callgraph-based cache analysis [x86 only]
- **MAQAO**: Assembly instrumentation & optimization [x86-64 only]
- mpiP/mpiPview: MPI profiling tool and analysis viewer
- Open MPI: Integrated memory checking
- Open|SpeedShop: Integrated parallel performance analysis environment
- **Paraver/Dimemas/Extrae**: Event tracing, graphical trace visualization & analysis
- Rubik: Process mapping generation & optimization [BG only]
- SIONlib/Spindle: Optimized native parallel file I/O & shared library loading
- STAT: Stack trace analysis tools
- SysMon: Batch system monitor plugin for Eclipse PTP

Technologies and their integration



Disclaimer

Tools will ***not*** automatically make you, your applications or computer systems more productive.

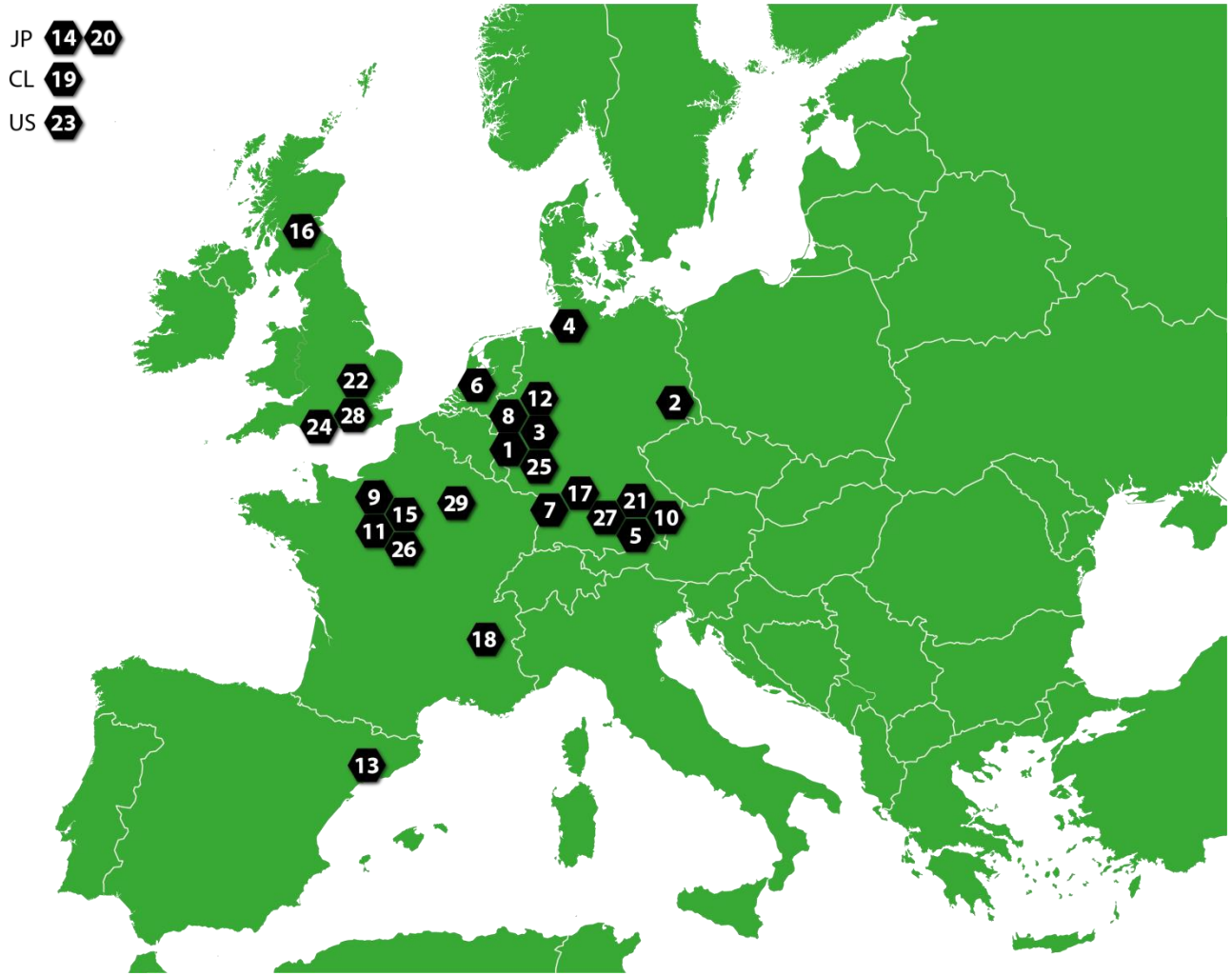
However, they can help you understand ***how*** your parallel code executes and ***when / where*** it's necessary to work on correctness and performance issues.

VI-HPS training & Tuning Workshops

- Goals
  - Give an overview of the programming tools suite
  - Explain the functionality of individual tools
  - Teach how to use the tools effectively
  - Offer hands-on experience and expert assistance using tools
  - Receive feedback from users to guide future development
- For best results, bring & analyze/tune your own code(s)!

- VI-HPS Hands-on Tutorial series
  - **SC**'08-11/13/14/15/16/17, ICCS'09, Cluster'10, EuroMPI'12/14, XSEDE'13, **ISC-HPC**'15-18
- VI-HPS Tuning Workshop series
  - 2008 (x2), 2009 (x2), 2010 (x2), 2011 (x2), 2012 (x2), 2013 (x2), 2014(x4)
  - 2015 (Stuttgart/Germany, Grenoble/France, Santiago/Chile)
  - 2016 (Kobe/Japan, Garching/Germany, Cambridge/UK, Livermore/USA)
  - 2017 (Southampton/UK, Aachen/Germany, Bruyères-le-Châtel/France)
  - 2018 (Garching/Germany, London/UK)

VI-HPS Tuning Workshop series



1. 2008/03/05+3: RWTH, Aachen, Germany
2. 2008/10/08+3: ZIH, Dresden, Germany
3. 2009/02/16+5: JSC, Jülich, Germany
4. 2009/09/09+3: HLRN, Bremen, Germany
5. 2010/03/08+3: TUM, Garching, Germany
6. 2010/05/26+3: SARA, Amsterdam, Netherlands
7. 2011/03/28+3: HLRS, Stuttgart, Germany
8. 2011/09/05+5: GRS, Aachen, Germany
9. 2012/04/23+5: UVSQ, St-Quentin, France
10. 2012/10/16+4: LRZ, Garching, Germany
11. 2013/04/22+4: MdS, Saclay, France
12. 2013/10/07+5: JSC, Jülich, Germany
13. 2014/02/10+5: BSC, Barcelona, Spain
14. 2014/03/25+3: RIKEN AICS, Kobe, Japan
15. 2014/04/07+4: MdS, Saclay, France
16. 2014/04/29+3: EPCC, Edinburgh, Scotland
17. 2015/02/23+5: HLRS, Stuttgart, Germany
18. 2015/05/18+5: UGA, Grenoble, France
19. 2015/10/27+3: NLHPC, Santiago, Chile
20. 2016/02/24+3: RIKEN AICS, Kobe, Japan
21. 2016/04/18+5: LRZ, Garching, Germany
22. 2016/07/06+3: Uni. Cambridge, England
23. 2016/07/27+3: LLNL, Livermore, California, USA
24. 2017/02/08+3: Uni. Southampton, England
25. 2017/03/27+5: RWTH, Aachen, Germany
26. 2017/10/16+5: Lab. ECR, Ter@tec, France
27. 2018/04/23+5: LRZ, Garching, Germany
28. 2018/06/21+3: UCL, London, England
29. 2018/10/15+5: ROMEO, Reims, France

Upcoming events

- 30th VI-HPS Tuning Workshop (21-25 January 2019, BSC, Barcelona, Spain)
- Further events to be determined
  - (one-day) tutorials: with guided exercises sometimes using a Live-ISO/OVA
  - (multi-day) training workshops: with your own applications on actual HPC systems
- Check **www.vi-hps.org/training** for announced events
- Contact us if you might be interested in hosting a training event