

MAQAO Performance Analysis and Optimization Tool



VI-HPS 27th Garching – Germany – 23-27 April 2018











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Introduction Performance analysis and optimisation

How much can I optimise my application?

- Can it actually be done?
- What would the effort/gain ratio be?

Where can I gain time?

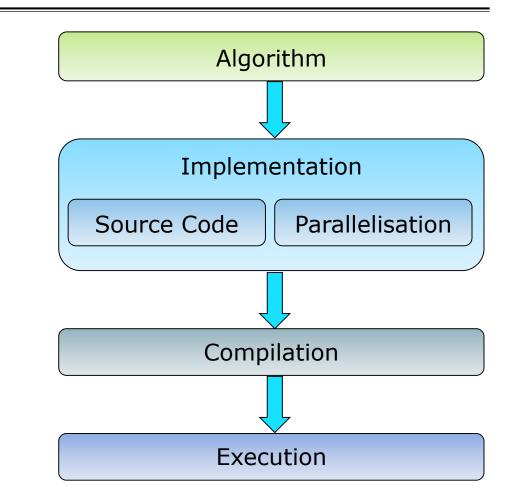
• Where is my application wasting time?

Why is the application spending time there?

- Algorithm, implementation or hardware?
- Data access or computation?

How can I improve the situation?

- In which step(s) of the design process?
- What additional information do I need?



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Introduction A multifaceted problem

Pinpointing the performance bottlenecks

Identifying the dominant issues

Algorithms, implementation, parallelisation, ...

Making the **best use** of the machine features

- Complex multicore and manycore CPUs
- Complex memory hierarchy

Finding the **most rewarding** issues to be fixed

- 40% total time, expected 10% speedup
 - ➡ TOTAL IMPACT: 4% speedup
- 20% total time, expected 50% speedup
 - → TOTAL IMPACT: 10% speedup

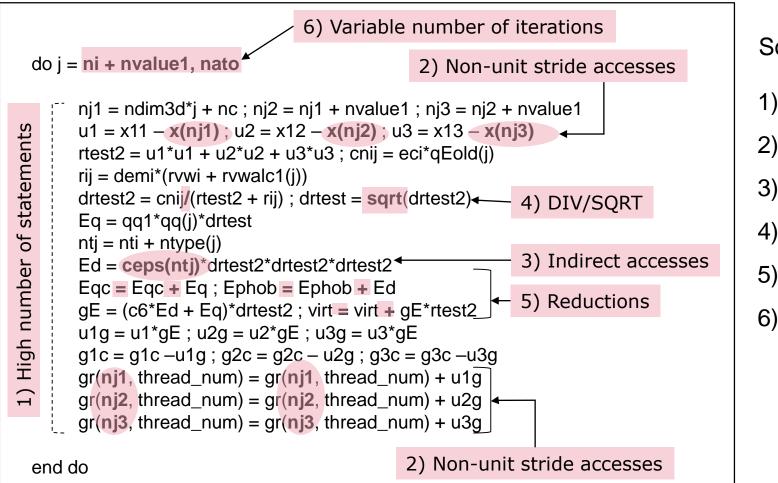


=> Need for dedicated and complementary tools

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Introduction *Motivating* example

Code of a loop representing ~10% walltime



Source code and associated issues:

- 1) High number of statements
- 2) Non-unit stride accesses
- 3) Indirect accesses
- 4) DIV/SQRT
- 5) Reductions
- 6) Variable number of iterations

Introduction MAQAO: Modular Assembly Quality Analyzer and Optimizer

Objectives:

- Characterizing performance of HPC applications
- Guiding users through optimization process
- Offering complementary views
- Estimating R.O.I.

Main features:

- Profiling
- Code quality analysis

Characteristics:

- Modular tool
- Support for Intel x86-64 and Xeon Phi
- LGPL3 Open Source software
- Developed at UVSQ since 2004



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Introduction Partnerships

MAQAO was funded by UVSQ, Intel and CEA (French department of energy) through Exascale Computing Research (ECR) and the French Ministry of Industry through various FUI/ITEA projects (H4H, COLOC, PerfCloud, ELCI, etc...)

Provides core technology to be integrated with other tools:

- TAU performance tools with MADRAS patcher through MIL (MAQAO Instrumentation Language)
- ATOS bullxprof with MADRAS through MIL
- Intel Advisor
- INRIA Bordeaux HWLOC

PeXL ISV also contributes to MAQAO:

- Commercial performance optimization expertise
- Training and software development

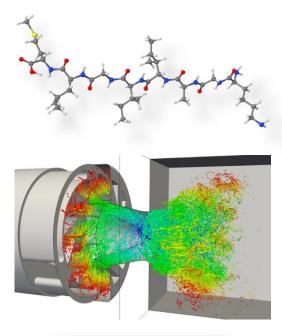


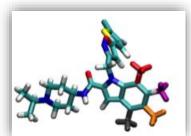
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Introduction Success stories

MAQAO was used for optimizing industrial and academic HPC applications:

- QMC=CHEM (IRSAMC)
 - Quantum chemistry
 - Speedup: > 3x
 - Moved invocation of function with identical parameters out of loop body
- Yales2 (CORIA)
 - Computational fluid dynamics
 - Speedup: up to 2.8x
 - Removed double structure indirections
- Polaris (CEA)
 - Molecular dynamics
 - Speedup: 1.5x 1.7x
 - Enforced loop vectorisation through compiler directives
- AVBP (CERFACS)
 - Computational fluid dynamics
 - Speedup: **1.08x 1.17x**
 - Replaced division with multiplication by reciprocal
 - Complete unrolling of loops with small number of iterations





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Introduction Some MAQAO Collaborators

- Prof. William Jalby
- Prof. Denis Barthou
- Prof. David J. Kuck
- Andrés S. Charif-Rubial, Ph D
- Jean-Thomas Acquaviva, Ph D
- Stéphane Zuckerman, Ph D
- Julien Jaeger, Ph D
- Souad Koliaï, Ph D
- Cédric Valensi, Ph D
- Eric Petit, Ph D
- Zakaria Bendifallah, Ph D
- Emmanuel Oseret, Ph D
- Pablo de Oliveira, Ph D

- Tipp Moseley, Ph D
- David C. Wong, Ph D
- Jean-Christophe Beyler, Ph D
- Mathieu Tribalat
- Hugo Bolloré
- Jean-Baptiste Le Reste
- Sylvain Henry, Ph D
- Salah Ibn Amar
- Youenn Lebras
- Othman Bouizi, Ph D
- José Noudohouenou, Ph D
- Aleksandre Vardoshvili
- Romain Pillot

Introduction MAQAO: Analysis at binary level

Advantages of binary analysis:

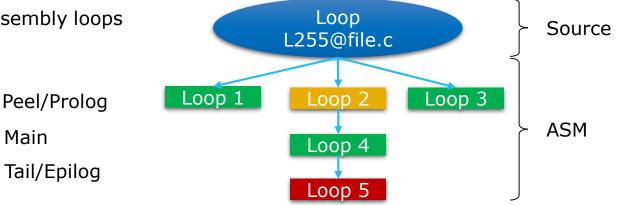
- Compiler optimizations increase the distance between the executed code and the source
- Source code instrumentation may prevent the compiler from applying some transformations

Main

We want to evaluate the "real" executed code: What You Analyse Is What You Run

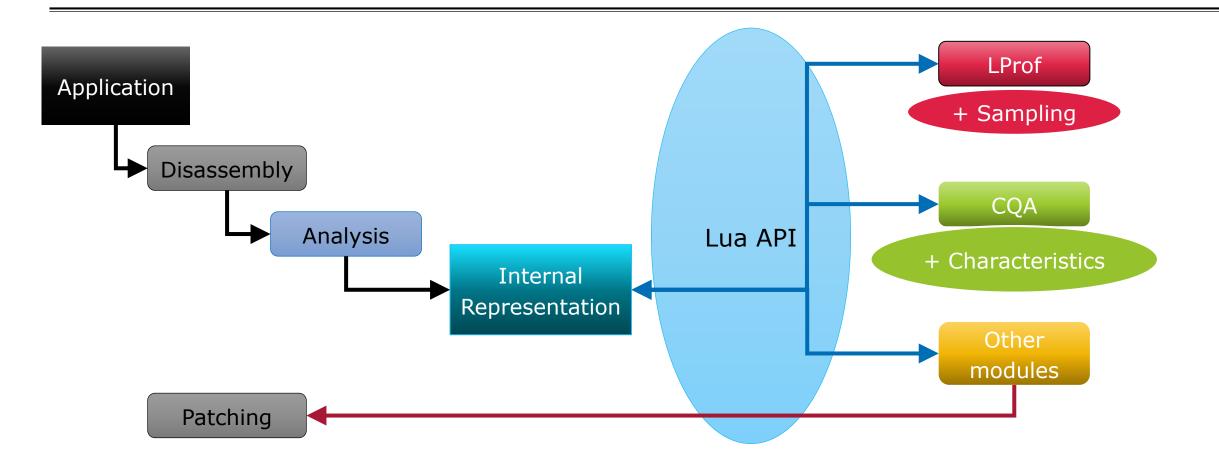
Main steps:

- Reconstruct the program structure
- Relate the analyses to source code
 - A single source loop can be compiled as multiple assembly loops
 - Affecting unique identifiers to loops



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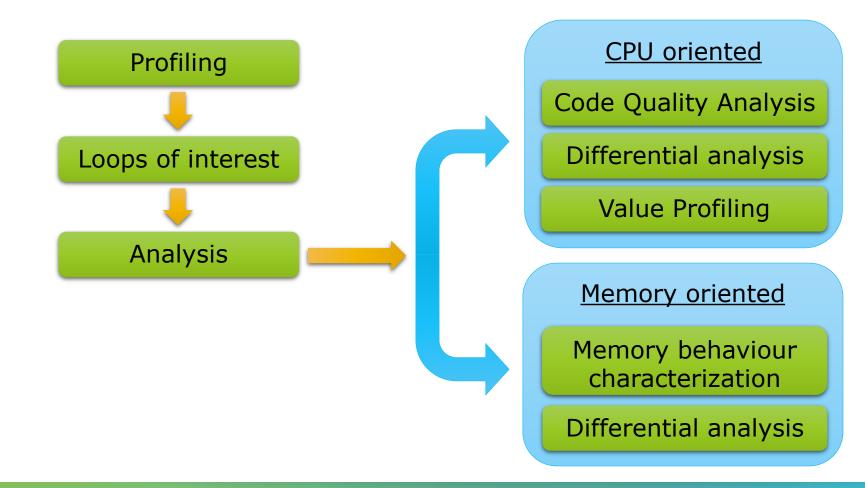
Introduction MAQAO Main structure



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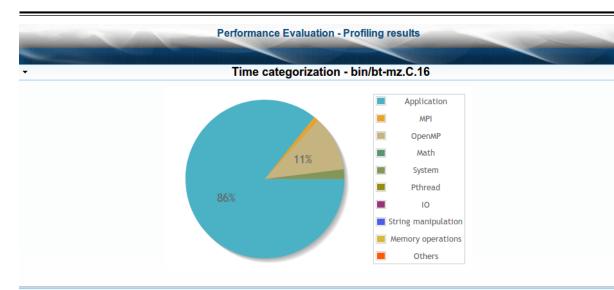
Introduction MAQAO Methodology

Decision tree



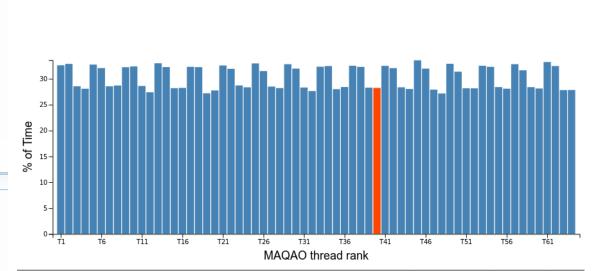
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MAQAO LProf: Lightweight Profiler



Hotspots - Functions

Name	Median Excl %Time	Deviation
pinvcrhs	30.06	4.87
▶ matmul_sub	13.19	1.02
<pre>INTERNAL_25src_kmp_barrier_cpp_3736d5c3::kmp_hyper_barrier_release(barrier_type, kmp_info*, int, int nt, void*)</pre>	, 11.3	50.92
z_solve	10.46	0.46
compute_rhs	8.87	0.48
y_solve	8.1	0.44
x_solve	7.91	0.41
matvec_sub	4.37	0.17
/IPIDI_CH3I_Progress	3.71	1.2
vinvrhs	0.59	0.02
_kmp_terminate_thread	0.56	0.11
Insinit	0.54	0.02
add#omp_loop_0	0.39	0.02



MAQAO LProf: Lightweight Profiler Introduction

Goal: Lightweight localization of application hotspots

Features:

- Sampling based
- Access to hardware counters for additional information
- Results at function and loop granularity

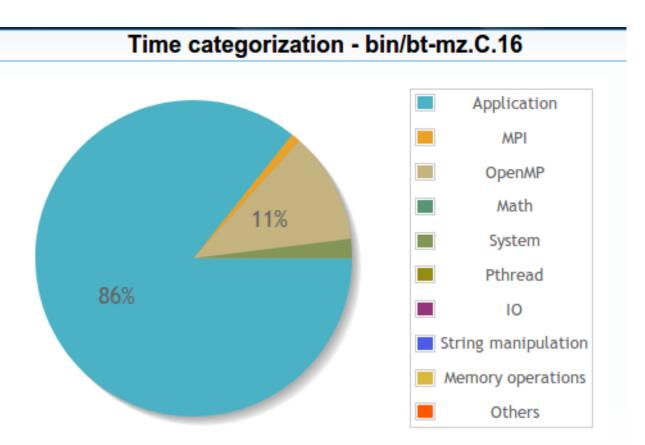
Strengths:

- Non intrusive: No recompilation necessary
- Low overhead
- Agnostic with regard to parallel runtime

MAQAO LProf: Lightweight Profiler Time categorization

Identifying at a glance where time is spent

- Application
 - Main executable
- Parallelization
 - Threads
 - OpenMP
 - MPI
- System libraries
 - I/O operations
 - String operations
 - Memory management functions
- External libraries
 - Specialised libraries such as libm / libmkl
 - Application code in external libraries





MAQAO LProf: Lightweight Profiler Functions hotspots

Focusing on user time:

Function hotspots

matmul_sub	5.05	8.97
z_solve	4.19	5.25
compute_rhs	3.28	3.89
▶ y_solve	3.1	3.67
x_solve	2.85	3.24
kmp_terminate_thread	2.1	1.27
matvec_sub	1.64	1.14
kmp_yield	0.73	0.17

MAQAO LProf: Lightweight Profiler Functions hotspots

Focusing on user time:

- Function hotspots
- Load balancing across the threads/processes/nodes

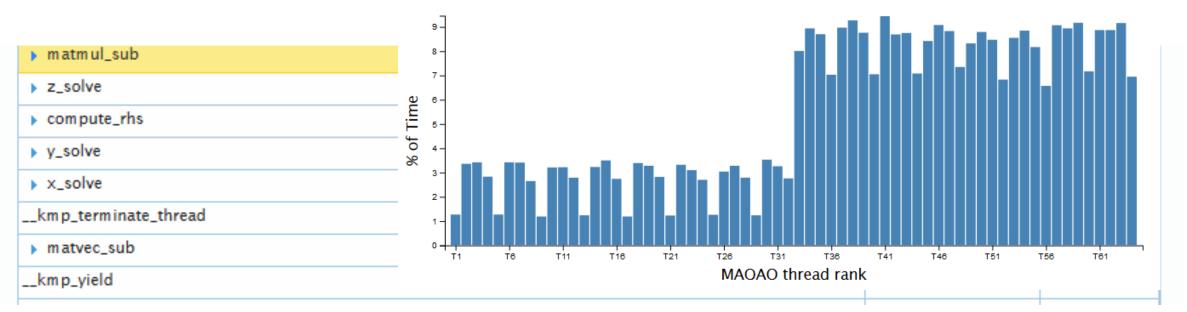
matmul_su	ıb	5.05	8.97
z_solve	Load balancing view	4.19	5.25
compute_	Load balanoing view	3.28	3.89
▶ y_solve	Sorted Load balancing view	3.1	3.67
x_solve		2.85	3.24
kmp_termii	Node view	2.1	1.27
matvec_su	b	1.64	1.14
kmp_yield		0.73	0.17

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MAQAO LProf: Lightweight Profiler Functions load balancing

Focusing on user time:

- Function hotspots
- Load balancing across the threads/processes/nodes

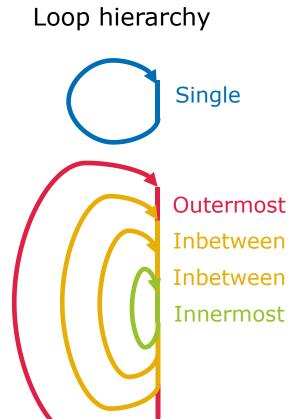


MAQAO LProf: Lightweight Profiler Loops hotspots

Analysing the time spent at loop level:

- Finding the most time consuming
- Providing loop id for further MAQAO analyses

▼ matmul_sub	5.05	8.97
✓ loops	2.92	2.95
o Loop 222 - solve_subs.f:71-175	0.5	0.11
o Loop 221 - solve_subs.f:71-175	2.44	1.95
✓ z_solve	4.19	5.25
✓ loops	4.19	5.24
Loop 223 - z_solve.f:53-423	0	0
Loop 225 - z_solve.f:54-423	0	0
Loop 228 - z_solve.f:54-423	0.06	0.02
o Loop 224 - z_solve.f:313-314	0.15	0.02
o Loop 227 - z_solve.f:55-137	1.4	0.7
 Loop 226 - z_solve.f:415-423 	0.73	0.19
 Loop 229 - z_solve.f:351-373 	0.06	0.02
o Loop 230 - z_solve.f:146-308	1.61	0.78



MAQAO CQA: Code Quality Analyzer

Characterize Control Contro Control Control	MA@AO						ASM	l code						
Norser	Code quality a	inalysis		In the binary file, the address of the loop	o is: 421	409		Loone						
• Source loop anding at line 37 in _/NPB3.3+M2/MP/BT-MZ/z_solve.f No VAPS SXXM13_SXM15 1 0.50 0.50 0 <th>The second se</th> <th></th> <th></th> <th>Instruction</th> <th>Nb Fl</th> <th>J PO</th> <th>P1</th> <th>P2</th> <th>P3</th> <th>P4</th> <th>P5</th> <th>P6</th> <th>Latency</th> <th>Recip. throughp</th>	The second se			Instruction	Nb Fl	J PO	P1	P2	P3	P4	P5	P6	Latency	Recip. throughp
• Surce loop anding at line 137 in _/NPB3.3-M2_MP/BT-MZ/z_solvesf 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	get processor is: Intel Xeon Phi Processor 3200, 5200, 7200 Series (x86_64/Kn	ghts Landing micro-architecture).		MOVAPS %XMM13,%XMM5	1	0.50	0.50	0	0	0	0	0	2	0.50
It is composed of the loop 227 MOVAPS \$XXMM15 \$\ldots 1 & 0.50 & 0.50 & 0 & 0 & 0 & 0 & 2 & 0.50 \\ MULSD \$XXMM15 \$\ldots XXMM15 \$\ldots 1 & 0.50 & 0.50 & 0 & 0 & 0 & 0 & 0 & 2 & 0.50 \\ MULSD \$XXMM15 \$\ldots XXMM15 \$\ldots XXMM15 \$\ldots 1 & 0.50 & 0.50 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 &				INC %RDI	1	0	0	0	0	1.50	0.50	0	1	1
MAQA Distance logic 227 Multip Stand Multip M	 Source loop ending at line 137 in/NPB3.3-MZ-MPI/B 	T-MZ/z_solve.f		DIVSD 0x28(%R10,%RDX,1),%XMM5	4	1	0	0.50	0.50	0	0	0	40-42	12-32
MQAO binary loop id: 227 MULSB XXMM15, xXMM15 1 0.50 0.50 0	It is composed of the loop 227			MOVAPS %XMM5,%XMM15	1	0.50	0.50	0	0	0	0	0	2	0.50
The loop is defined in /tmp/WPB3.31.MZ/WPJSTMZ/z_solveL55:137 MOVSD SXMMA(S, 0X12890(RR14)) 1 0 0 0.0 0 0 1 2 1 2% of pack computational performance is used (0.79 out of 3.20 FLOP per cycle (CFLOPS # 1CH2)) MOVSD SXMMA(S, 0X12890(RR14)) 1 0.0 0.0 0 1 2 1 2% of pack computational performance is used (0.79 out of 3.20 FLOP per cycle (CFLOPS # 1CH2)) Vector isstit (Fight and Sign and				MULSD %XMM5,%XMM15	1	0.50	0.50	0	0	0	0	0	6	0.50
2% of peak computational performance is used 0.79 out of 32.00 FLOP per cycle (GFLOPS # 1GH2) 1 0.90 0.90 0.90 0	· · · ·	1. 075 407		MOVSD %XMM5,0x12890(%R14)	1	0	0	0.50	0.50	0	0	1	2	1
Cain Potential gain Hints Experts only Vectorizatio Your loop is probably not vectorizatio Vectorizatio 13% 12 Your loop is probably not vectorizatio 13% 0 12 Your loop is probably not vectorizatio 15% 0 12 1 Note your control of the scale of an isotation from 30% 12% 1 2 1 Store of and antiverse of scale of any loop reset of the scale of any loop reset of any loop reset of the scale of any loop reset of any lo				MULSD %XMM15,%XMM5	1	0.50	0.50	0	0	0	0	0	6	0.50
Vector Vector<		FLOP per cycle (GFLOPS @ 1GHz))		MOVSD %XMM15,0x12898(%R14)	1	0	0	0.50	0.50	0	0	1	2	1
Vectorizatio all 13% 0 0 1 2 1 Vort log table rot-predity instructions are used in scalar version pg indd 15% 0 0 1 2 1 Store log redity instructions are used in scalar version pg indd 15% 0 0 1 2 1 Store log redity instructions are used in scalar version pg instruction 15% 0 0 1 2 1 (interview) instruction star version pg instruction 15% 0 0 1 2 1 (interview) interview instruction	Gain Potential gain Hints Experts only		Vector effi	iciency ratios						0	0	1	2	1
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store and arithmetical SSFAX instructions are used in scalar version (a i	Only 13% of vector register length is used (average across all SSE/AVX in			1 5%						0	0	1	2	1
Source and arithmetical SSLAVX instructions are used in scalar version (i) 0 0 1 2 1 Since your section units section units and in version (i) 12% 0 0 0 5 0.50 In ull 12% 12% 0 0 0 5 0.50 In ull 12% 12% 0 0 0 5 0.50 In ull 12% 12% 0 0 0 5 0.50 In ull 0 12% 0 0 0 5 0.50 In ull 0 12% 0 <		storo		12%						0	0	1	2	1
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• Try another compiler or update/tune your current one: 0		indi								0	0	0	5	0.50
• use the vec-report option to understand why your loop was • Normal metric actions dependences from your loop and make to • Remove inter-iterations dependences from your loop and make to • Of your arrays have 2 or more dimensions, check whether if • of ty our arrays have 2 or more dimensions, check whether if • of ty our arrays have 2 or more dimensions, check whether if • of ty our arrays of structures (kos), try to use stru- • of ty our arrays of structures (kos), try to use stru- • of ty our arrays of structures (kos), try to use stru- • d's of peak load performance is reached (5.13 out of 128.00 bytes loaded per cycle (CB/s @ 1CHz)) • of ty our loop streams arrays of structures (kos), try to use stru- • d's of peak load performance is reached (4.61 out of 64.00 bytes stored per cycle (CB/s @ 1CHz)) • 7% of peak store performance is reached (4.61 out of 64.00 bytes stored per cycle (CB/s @ 1CHz)) • 7% of peak store performance is reached (4.61 out of 64.00 bytes stored per cycle (CB/s @ 1CHz)) • 7% of peak store performance is reached (4.61 out of 64.00 bytes stored per cycle (CB/s @ 1CHz)) • 7% of peak store performance is reached (4.61 out of 64.00 bytes stored per cycle (CB/s @ 1CHz)) • 7% of peak store performance is limited by instruction throughput (loading/decoding program instructions to execution core) (front-end is a • 0 0 1 2 1 • 0 0 0 5 0.50 • 0 0 0 5 0.50	 Try another compiler or undate/tune your current one: 									0	0	0	5	0.50
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• of fyour arrays have 2 or more dimensions, check whether el 0										0	0	0	5	0.50
Fortran storage order is column-major: do i do j a(i,j) = b(i,j) Assuming all data it into the L1 cache, each iteration of the binary loop takes 92.00 cycles. At this rate. 0 0 1 2 1 0 0 i a()(%x = b()(%x (slow, non stride 1) => do i a%x(i) = b%x(i) - 4% of peak load performance is reached (5.13 out of 128.00 bytes loaded per cycle (CB/s @ 1GHz)) 0			cles and memo	ory resources usage						0	0	0	6	0.50
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do i a(1)%x = b(1)%x (slow, non stride 1) => do i a%x(1) = b%x(1) • 7% of peak store performance is reached (4.61 out of 64.00 bytes stored per cycle (GB/s @ 1GHz)) 0 0 0 0 0 0 1 2 1 • 7% of peak store performance is reached (4.61 out of 64.00 bytes stored per cycle (GB/s @ 1GHz)) • 7% of peak store performance is reached (4.61 out of 64.00 bytes stored per cycle (GB/s @ 1GHz)) 0 0 0 1 2 1 • Front-end bottlenecks • 7% of peak store performance is reached (4.61 out of 64.00 bytes stored per cycle (GB/s @ 1GHz)) 0 0 0 1 2 1 • Source loop ending at line 308 in/NPB3.3-MZ-MPI/BT • Source loop ending at line 314 in/NPB3.3-MZ-MPI/BT • O 0 0 0 0 0 1 2 1 • Source loop ending at line 373 in/NPB3.3-MZ-MPI/BT • MOV3D #AMINI #,UA40(MK-3,#KL +,1) • O 0 0 0 0 1 2 1 • Source loop ending at line 373 in/NPB3.3-MZ-MPI/BT • MOV3D #AMINI #,UA40(MK-3,#KL +,1) • O 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										0	0	1	2	1
Execution units bot Found no such bottlenecks but see expert reports for more complex bott Performance is limited by instruction throughput (loading/decoding program instructions to execution core) (front-end is a bottleneck). Source loop ending at line 308 in/NPB3.3-MZ-MPI/BT Performance is limited by instruction throughput (loading/decoding program instructions to execution core) (front-end is a bottleneck). Source loop ending at line 314 in/NPB3.3-MZ-MPI/BT MOVSD 7xAMM1+1, VX40(VXD-7,7KL+1,1) 0 0 0.50 0.50 Source loop ending at line 373 in/NPB3.3-MZ-MPI/BT MOVSD 7xAMM1+1, VX40(VXD-7,7KL+1,1) 0 0 0.50 0.50 Source loop ending at line 373 in/NPB3.3-MZ-MPI/BT MOVSD 7xAMM1+1, VX40(VXD-7,7KL+1,1) 0 0 0.50 0.50 0 0 1 2 1 MOVSD 0x12898(%R14),%XMM2 1 0 0 0.50 0.50 0 0 0.50 0.50										0	0	0	5	0.50
Execution units bot Found no such bottlenecks but see expert reports for more complex but Found no such bottlenecks but see expert reports for more complex but Front-end bottlenecks 0 0 1 2 1 Source loop ending at line 308 in/NPB3.3-MZ-MPI/BT Performance is limited by instruction throughput (loading/decoding program instructions to execution core) (front-end is a bottleneck). 0	do I a(1)%x = D(1)%x (slow, non stride I) => $do I a%x(I) = D%x(I)$	 7% of peak store performance is reached 	ed (4.61 out of 64.0	00 bytes stored per cycle (GB/s @ 1GH	łz))					0	0	0	6	0.50
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> Source loop ending at line 314 in/NPB3.3-MZ-MPI/B1-MZ/Z_solve.f MOVSD 0x38(%R10,%RDX,1),%XMM3 1 0 0 0.50 0 1 2 1 > Source loop ending at line 373 in/NPB3.3-MZ-MPI/BT-MZ/z_solve.f MOVSD 0x38(%R10,%RDX,1),%XMM3 1 0 0 0.50 0 0 5 0.50 Source loop ending at line 373 in/NPB3.3-MZ-MPI/BT-MZ/z_solve.f MOVSD 0x12898(%R14),%XMM2 1 0 0 0.50 0 0 5 0.50			ughput (loading/de	ecoding program instructions to exe	ecutior	core)	(front-	end is	a	0	0	0	6	0.50
> Source loop ending at line 373 in/NPB3.3-MZ-MPI/BT-MZ/z_solve.f MOVSD 0x38(%R10,%RDX,1),%XMM3 1 0 0 0.50 0.50 0 0 5 0.50 Source loop ending at line 373 in/NPB3.3-MZ-MPI/BT-MZ/z_solve.f MOVSD 0x38(%R10,%RDX,1),%XMM3 1 0 0 0.50 0.50 0 0 5 0.50	Source loop ending at line 308 in/NPB3.3-MZ-MPI/B	bottleneck).								0	0	1	2	1
Source loop ending at the 375 ft and 1055 ft an	Source loop ending at line 314 in/NPB3.3-MZ-MPI/B	I-MZ/Z_SOIVE.T		MOVOD 70AMM14,0X46(70K3,70K14,1)	1	v	v	0.50	0.50	0	0	1	2	1
	Source loop ending at line 373 in/NPB3.3-MZ-MPI/B	T-MZ/z_solve.f		MOVSD 0x38(%R10,%RDX,1),%XMM3	1	0	0	0.50	0.50	0	0	0	5	0.50
MULSD %XMM3,%XMM2 1 0.50 0.50 0 0 0 0 6 0.50	Course loop anding at line 400 in _/NDD2 2 M7 MDI /D	T M7 /= coluct	_	MOVSD 0x12898(%R14),%XMM2	1	0	0	0.50	0.50	0	0	0	5	0.50
				MULSD %XMM3,%XMM2	1	0.50	0.50	0	0	0	0	0	6	0.50

MAQAO CQA: Code Quality Analyzer Introduction

Goal: Assist developers in improving code performance

Features:

- Evaluates the quality of the compiler generated code
- Returns hints and workarounds to improve quality
- Focuses on loops
 - In HPC most of the time is spent in loops
- Targets compute-bound codes

Static analysis:

- Requires no execution of the application
- Allows cross-analysis

MAQAO CQA: Code Quality Analyzer Processor Architecture: Core level

Most of the time, applications only exploit at best 5 to 10% of the peak performance.

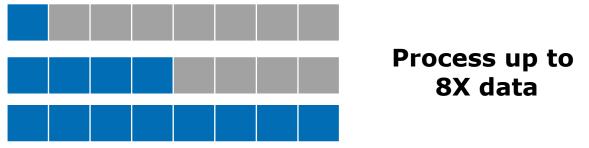
Main elements of analysis:

- Peak performance
- Execution pipeline
- Resources/Functional units

Key performance levers for core level efficiency:

- Vectorizing
- Avoiding high latency instructions if possible
- Having the compiler generate an efficient code

Same instruction – Same cost



MAQAO CQA: Code Quality Analyzer Output

High level reports:

- Reference to the source code
- Bottleneck description
- Hints to improve performance
- Reports categorized by confidence level
 - gain, potential gain

Low level reports for performance experts

- Assembly-level
- Instructions cycles costs
- Instructions dispatch predictions

Source loop ending at line 137 in .../NPB3.3-MZ-MPI/BT-MZ/z_solve.f

It is composed of the loop 227

MAQAO binary loop id: 227

The loop is defined in /tmp/NPB3.3.1-MZ/NPB3.3-MZ-MPI/BT-MZ/z_solve.f:55-137

2% of peak computational performance is used (0.79 out of 32.00 FLOP per cycle (GFLOPS @ 1GHz))

Gain Potential gain Hints Experts only

Vectorization

Your loop is probably not vectorized.

Only 13% of vector register length is used (average across all SSE/AVX instructions).

By vectorizing your loop, you can lower the cost of an iteration from 92.00 to 12.13 cycles (7.59x speedup).

Store and arithmetical SSE/AVX instructions are used in scalar version (process only one data element in vector registers). Since your execution units are vector units, only a vectorized loop can use their full power.

Proposed solution(s):

Try another compiler or update/tune your current one:

use the vec-report option to understand why your loop was not vectorized. If "existence of vector dependences", try
the IVDEP directive. If, using IVDEP, "vectorization possible but seems inefficient", try the VECTOR ALWAYS directive.

- Remove inter-iterations dependences from your loop and make it unit-stride:
 - If your arrays have 2 or more dimensions, check whether elements are accessed contiguously and, otherwise, try to permute loops accordingly.

Fortran storage order is column-major: do i do j a(i,j) = b(i,j) (slow, non stride 1) => do i do j a(j,i) = b(i,j) (fast, stride 1)

 If your loop streams arrays of structures (AoS), try to use structures of arrays instead (SoA): do i a(i)%x = b(i)%x (slow, non stride 1) => do i a%x(i) = b%x(i) (fast, stride 1)

MAQAO CQA: Code Quality Analyzer Compiler and programmer hints

Compiler can be driven using flags and pragmas:

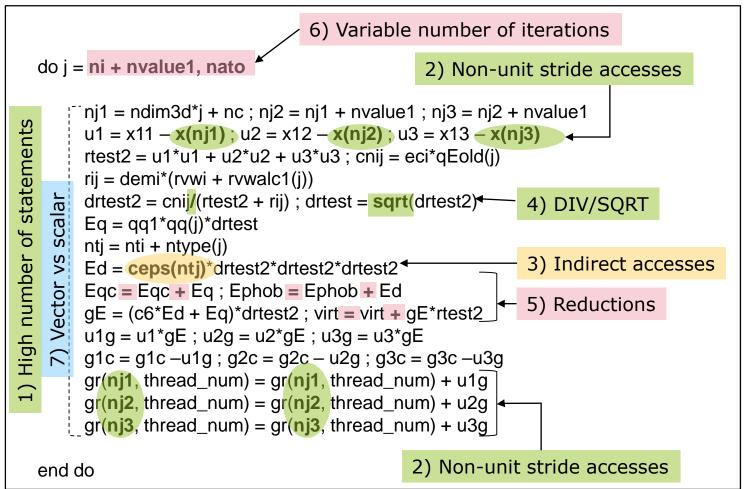
- Ensuring full use of architecture capabilities (e.g. using flag -xHost on AVX capable machines)
- Forcing optimization (unrolling, vectorization, alignment, ...)
- Bypassing conservative behaviour when possible (e.g. 1/X precision)

Implementation changes:

- Improve data access
 - Loop interchange
 - Changing loop strides
- Avoid instructions with high latency

MAQAO CQA: Code Quality Analyzer Application to motivating example

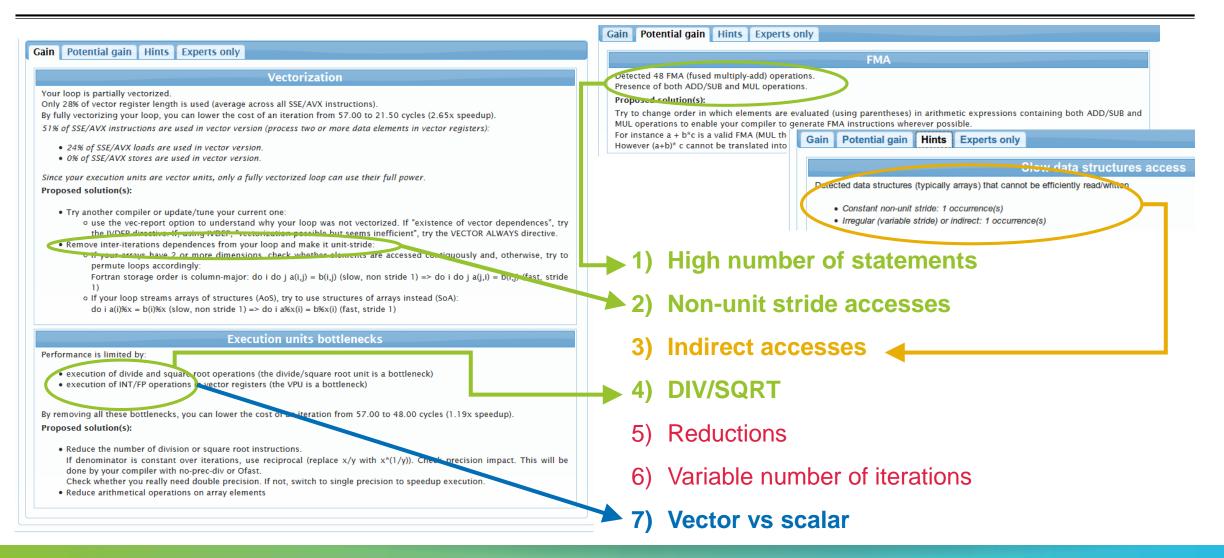
Issues identified by CQA



CQA can detect and provide hints to resolve most of the identified issues:

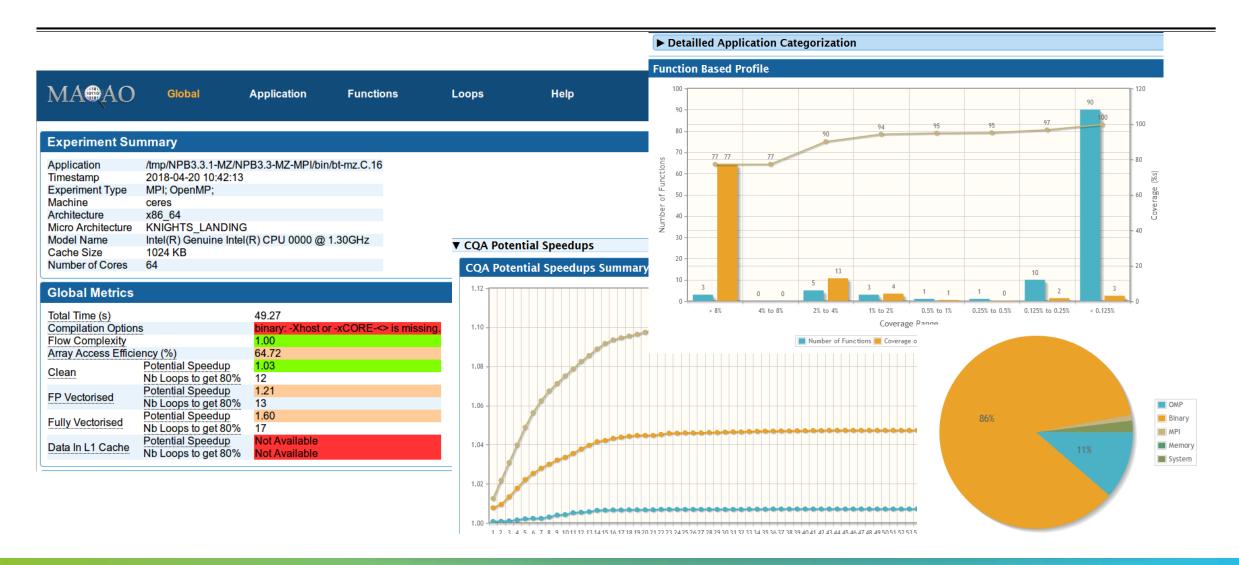
- 1) High number of statements
- 2) Non-unit stride accesses
- 3) Indirect accesses
- 4) DIV/SQRT
- 5) Reductions
- 6) Variable number of iterations
- 7) Vector vs scalar

MAQAO CQA: Code Quality Analyzer Application to motivating example



VIRTUAL INSTITUTE - HIGH PRODUCTIVITY SUPERCOMPUTING

MAQAO ONE View: Performance View Aggregator

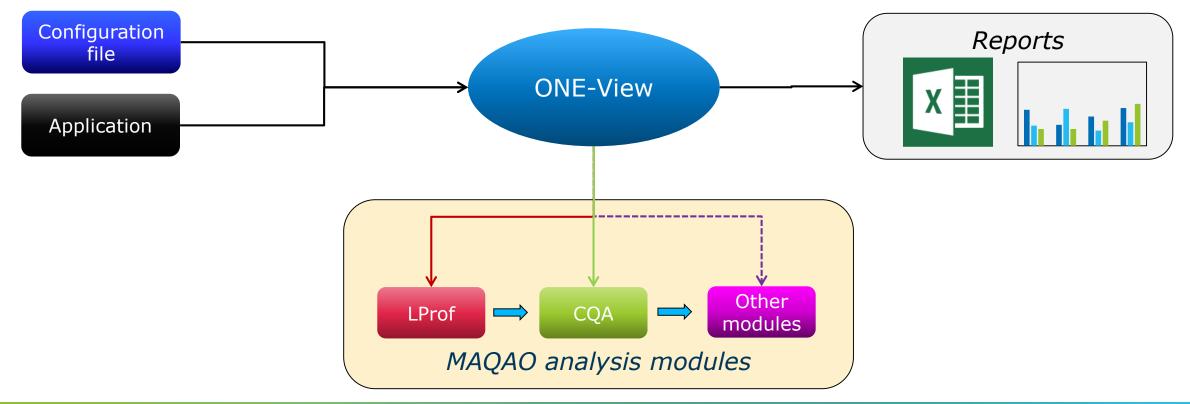




MAQAO ONE View: Performance View Aggregator *Introduction*

Automating the full analysis process

- Invocation of the MAQAO modules
- Generation of aggregated performance views as HTML or XLS graphs

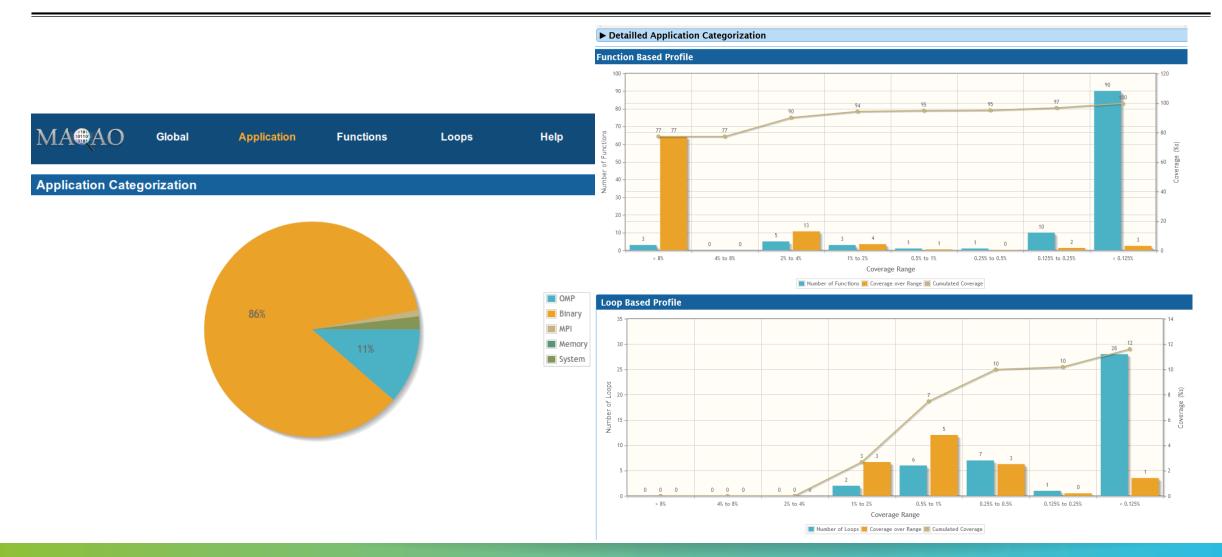


V VIRTUAL INSTITUTE - HIGH PRODUCTIVITY SUPERCOMPUTING

MAQAO ONE View: Performance View Aggregator GUI sample: Global View



MAQAO ONE View: Performance View Aggregator GUI sample: Application Characteristics



V VIRTUAL INSTITUTE - HIGH PRODUCTIVITY SUPERCOMPUTING

MAQAO ONE View: Performance View Aggregator GUI sample: Functions and Loops Views

						X	70			
inctions and Loops						Loops Inde	ex			
pt-click on a line to display the associated load balancing. uble click on a loop to display its analysis details.						Double click o	n a loop to	display its analysis details.		
Name	Module	Coverage (%)	Time (s)	Nb Threads	Deviation	Loop id	Source Lines	Source File	Source Function	Cov (
binvcrhs	binary	30.34	15.02	64	2.24	Loop 224	71-175	binary:solve_subs.f	matmul_sub	6
matmul sub	binary	13.25	6.55	64	0.93	Loop 233	146-308	binary:z_solve.f	z_solve	3
 Loop 224 - solve subs.f:71-175 - binary 	billary	6.07	3	04	0.33	Loop 230	55-137	binary:z_solve.f	z_solve	3
 Loop 225 - solve_subs.f.71-175 - binary Loop 225 - solve_subs.f.71-175 - binary 		1.36	0.67			Loop 200			x_solve	:
z solve	binary	10.54	5.21	64	0.68	Loop 207	145-307	binary:y_solve.f	y_solve	_
INTERNAL 25 src kmp barrier cpp 3736d5c3:: kmp hyper barrier release						Loop 204	55-137	binary:y_solve.f	y_solve	
int_Entval_25stc_ntp_barter_cpp_57500565kttp_ttyper_barter_release	libiomp5.so	9.84	4.87	64	7.04	Loop 197	57-139	binary:x_solve.f	x_solve	_
compute rhs	binary	8.93	4.42	64	0.64	Loop 229 Loop 122	415-423 304-349	binary:z_solve.f binary:rhs.f	z_solve	
y solve	binary	8.07	3.99	64	0.65	Loop 122 Loop 148	304-349 194-238	binary:rhs.f	compute_rhs compute_rhs	
x solve	binary	7.88	3.9	64	0.65	Loop 148	395-399	binary:x solve.f	x solve	
matvec sub	binary	4.5	2.23	64	0.40	Loop 225	71-175	binary:solve subs.f	matmul sub	
MPIDI CH3I Progress	libmpi.so.12.0	0.89	0.44	16	0.94	Loop 162	83-132	binary:rhs.f	compute rhs	
binyrhs	binary	0.6	0.3	64	0.06	Loop 221	23-27	binary:solve subs.f	matvec sub	
• Ihsinit	,		0.0		0.00	Loop 203	394-398	binary:y solve.f	y solve	
kmp terminate thread	binary - Lo	oop 224				Loop 223	23-27	binary:solve subs.f	matvec sub	
add#omp loop 0						Loop 170	40-50	binary:rhs.f	compute rhs	
		_				Loop 227	313-314	binary:z solve.f	z solve	
np info*, int, int, void (*)(void*, void*), void*)						Loop 105	388-391	binary:rhs.f	compute rhs	
kmp yield						Loop 206	337-360	binary:y solve.f	y solve	
copy x face#omp loop 0 5.5-						Loop 166	65-67	binary:rhs.f	compute rhs	
						Loop 236	26-28	binary:add.f	add#omp loop 0	
exact solution						Loop 199	342-364	binary:x solve.f	x solve	
task tick fair 4.5 -						Loop 12	227-234	binary:initialize.f	Ihsinit	
						Loop 155	157-160	binary:rhs.f	compute rhs	
copy x face#omp loop 1						Loop 222	23-27	binary:solve subs.f	matvec sub	
apic timer interrupt						Loop 130	265-268	binary:rhs.f	compute_rhs	
rcu_check_callbacks g, 40- copy_x_face#omp_loop_1 g; 3.5- apic_timer_interrupt b; 3.0-						Loop 92	431-433	binary:rhs.f	compute_rhs	
trigger load balance						Loop 232	351-373	binary:z_solve.f	z_solve	
ktimo got						Loop 214		binary:exch_qbc.f	copy_x_face#omp_loop_0	
copy y face#omp loop 1						Loop 218	207-209	binary:exch_qbc.f	copy_y_face#omp_loop_0	
hrtimer_run_queues						Loop 107	388-391	binary:rhs.f	compute_rhs	
ktime_get_update_offsets_now						Loop 36	19-23	binary:exact_solution.f	exact_solution	_
run timer softira						Loop 140	265-268	binary:rhs.f	compute_rhs	
clear page c e						Loop 160	139-151	binary:rhs.f	compute_rhs	_
exact rhe#omn region 0						Loop 216	258-260	binary:exch_qbc.f	copy_x_face#omp_loop_1	

MAQAO ONE View: Performance View Aggregator GUI sample: CQA Output

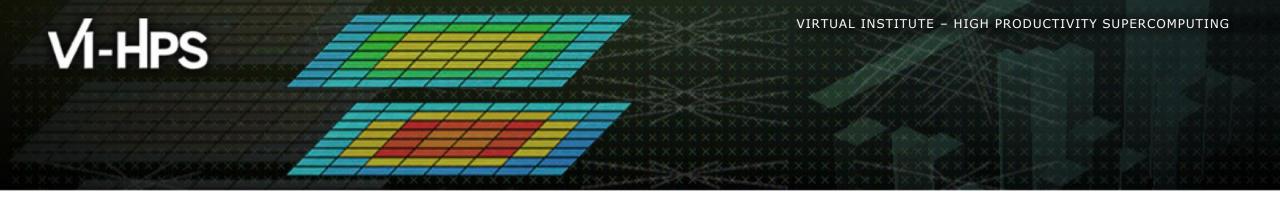
		Static Reports
		▼ CQA Report
		The loop is defined in /tmp/NPB3.3.1-MZ/NPB3.3-MZ-MPI/BT-MZ/z_solve.f:415-423
		▼ Path 1
MAC Global Application Functions	Loops Help	2% of peak computational performance is used (0.77 out of 32.00 FLOP per cycle (GFLOPS @ 1GHz)) gain potential hint expert
Loop 226		Code clean check
Coverage 0.51 %		Detected a slowdown caused by scalar integer instructions (typically used for address computation). By removing them, you can lower the cost of an iteration from 65.00 to 57.00 cycles (1.14x speedup).
Function z_solve		Workaround
Source file and lines z_solve.f:415-423		• Try to reorganize arrays of structures to structures of arrays
Module binary		 Consider to permute loops (see vectorization gain report) To reference allocatable arrays, use "allocatable" instead of "pointer" pointers or qualify them with the
▼ Source Code		"contiguous" attribute (Fortran 2008) • For structures, limit to one indirection. For example, use a_b%c instead of a%b%c with a_b set to a%b
/tmp/NPB3.3.1-M2/NPB3.3-M2-MPI/BT-M2//z_solve.f: 415 - 423		before this loop
415: do k=ksize-1,0,-1		Vectorization
416: do m=1,BLOCK_SIZE 417: do n=1,BLOCK_SIZE		Your loop is not vectorized. 8 data elements could be processed at once in vector registers. By vectorizing your
418: rtmp(m,k) = rtmp(m,k) 419: > - lhs(m,n,cc,k)*rtmp(n,k+1) 420: enddo		loop, you can lower the cost of an iteration from 65.00 to 8.12 cycles (8.00x speedup).
421: rhs(m,i,j,k) = rtmp(m,k) 422: enddo		
423: enddo 424:		Try another compiler or update/tune your current one: o use the vec-report option to understand why your loop was not vectorized. If "existence of vector
425: enddo 426: enddo		dependences", try the IVDEP directive. If, using IVDEP, "vectorization possible but seems inefficient", try the VECTOR ALWAYS directive.
		Remove inter-iterations dependences from your loop and make it unit-stride:
Assembly Code		otherwise, try to permute loops accordingly: Fortran storage order is column-major: do i do j $a(i,j) = b(i,j)$ (slow, non stride 1) => do i do j $a(j,i) = b(i,j)$ (fast, stride 1)
		 If your loop streams arrays of structures (AoS), try to use structures of arrays instead (SoA): do i a(i)%x = b(i)%x (slow, non stride 1) => do i a%x(i) = b%x(i) (fast, stride 1)
		Execution units bottlenecks
		Found no such bottlenecks but see expert reports for more complex bottlenecks.

MAQAO ONE View: Performance View Aggregator GUI sample: Advanced Loop Metrics

ther static metrics		▼ Memory Groups
Advanced static metrics		0x422a97 MOVSD 0x11d50(%R11,%RCX,1),%XMM7 [3]
▼ Path 1		0x422aa1 INC %R10
V Path I		0x422aa4 MOVSD 0x73a0(%RSI,%RDX,1),%XMM8 [2]
Metric	Value	0x422aae MULSD %XMM7,%XMM8
Coverage (% app. time)	0.51	0x422ab3 MOVSD 0x11d28(%R11,%RCX,1),%XMM13 [3]
Time (s)	0.24	0x422abd MOVSD 0x11d58(%R11,%RCX,1),%XMM6 [3]
CQA speedup if clean	1.14	0x422ac7 SUBSD %XMM8,%XMM13
CQA speedup if FP arith vectorized	1.66	0x4 Size: 25
CQA speedup if fully vectorized	8.00	Oxi Pattern: LLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLL
CQA speedup if no inter-iteration dependency	NA	0x Span: 200
CQA speedup if next bottleneck killed	1.02	0x Head: 0 [3]
Source	z_solve.f:415-423	0x. Unroll factor: 5
Source loop unroll info	not unrolled or unrolled with no peel/tail loop	0x Stride status: Success Stride: -600
Source loop unroll confidence level	max	Ox Accessed memory status: Success 2]
Unroll/vectorization loop type	NA	0x Accessed memory: 200
Unroll factor	NA	0x Accessed memory without overlapping: 200 [3]
CQA cycles	65.00	Ox. Accessed memory reused: 0
CQA cycles if clean	57.00	0x422b1c MOVSD %XMM15,0x11d28(%R11,%RCX,1) [3]
CQA cycles if FP arith vectorized	39.23	0x422b26 MOVSD 0x7418(%RSI,%RDX,1),%XMM11 [2]
CQA cycles if fully vectorized	8.12	0x422b30 MULSD %XMM4,%XMM11
Front-end cycles	65.00	0x422b35 MOVSD 0x11d70(%R11,%RCX,1),%XMM3 [3]
P0 cycles	25.00	0x422b3f SUBSD %XMM11,%XMM13
P1 cycles	25.00	0x422b44 MOVSD %XMM13,0x11d28(%R11,%RCX,1) [3]
P2 cycles	35.00	0x422b4e MOVSD 0x7440(%RSI,%RDX,1),%XMM12 [2]
P3 cycles	35.00	0x422b58 MULSD %XMM3,%XMM12
P4 cycles	4.50	0x422b5d MOVSD 0x11d30(%R11,%RCX,1),%XMM10 [3]
P5 cycles	4.50	0x422b67 SUBSD %XMM12,%XMM13
P6 cycles	30.00	0x422b6c MOVSD %XMM13,0x11d28(%R11,%RCX,1) [3]
P7 cycles	NA	0x422b76 MOVSD 0x73a8(%RSI,%RDX,1),%XMM14 [2]
DIV/SQRT cycles	0.00	0x422b80 MULSD %XMM7,%XMM14
Inter-iter dependencies cycles	1	0x422b85 MOV 0x11d28(%R15,%R14,1),%R13 [4]
Nb insns	128	0x422b8d SUBSD %XMM14,%XMM10
		0x422b92 MOVSD %XMM10,0x11d30(%R11,%RCX,1) [3]

MAQAO ONE View: Performance View Aggregator GUI sample: Help

	on <u>the MAQAO website</u> .
▼ Help about "C	
The Global tab is	e report index and it presents several sections:
Charts in CC • If Code include • If FP Vo • If Fully All sections • One su • At least corresp The last sect	Initial Speedups charts need that LPROF and CQA modules are available in MAQAO and enabled in the report; Potential Speedups present speedups obtainable if the assembly code is modified to satisfy some conditions: Ilean means that all instructions which do not perform floating-point computation or memory accesses are deleted. Instructions used to handle the loop control flow are not in the instructions set to remove. torized means that all instructions performing floating-point computation are vectorized ectorized means that all instructions performing floating-point computation and all memory accesses are vectorized. Intain two types of charts: mary chart where the X axis represents the number of loops to modify in order to obtain the speedup; ne ordered chart where the X axis represents loops identifiers to modify in order to obtain the speedup. The speedup. In contains all parameters from the experiment configuration file.
	plication" tab
▼ Help about "A	



Thank you for your attention !

Questions ?

