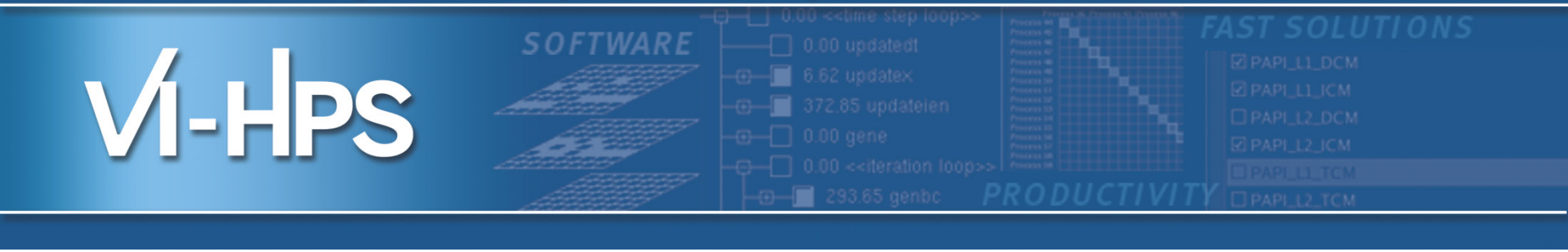


Introduction to VI-HPS

Brian Wylie
Jülich Supercomputing Centre

Goal: Improve the quality and accelerate the development process of complex simulation codes running on highly-parallel computer systems

- Start-up funding (2006–2011) by Helmholtz Association of German Research Centres

- Activities
  - Development and integration of HPC programming tools
    - Correctness checking & performance analysis
  - Training workshops
  - Service
    - Support email lists
    - Application engagement
  - Academic workshops

http://www.vi-hps.org

VI-HPS partners (founders)

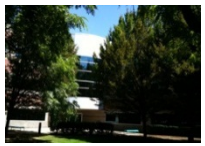



- Forschungszentrum Jülich
  - Jülich Supercomputing Centre
- RWTH Aachen University
  - Centre for Computing & Communication
- Technical University of Dresden
  - Centre for Information Services & HPC
- University of Tennessee (Knoxville)
  - Innovative Computing Laboratory

VI-HPS partners (cont.)







- Barcelona Supercomputing Center
  - Centro Nacional de Supercomputación
- German Research School
  - Laboratory of Parallel Programming
- Lawrence Livermore National Lab.
  - Centre for Applied Scientific Computing
- Technical University of Munich
  - Chair for Computer Architecture
- University of Oregon
  - Performance Research Laboratory
- University of Stuttgart
  - HPC Centre
- University of Versailles St-Quentin
  - LRC ITACA

Productivity tools

MUST

- MPI usage correctness checking

PAPI

- Interfacing to hardware performance counters

Periscope

- Automatic analysis via an on-line distributed search

Scalasca

- Large-scale parallel performance analysis

TAU

- Integrated parallel performance system

Vampir

- Interactive graphical trace visualization & analysis

Score-P

- Community instrumentation & measurement infrastructure

Productivity tools (cont.)

KCachegrind
- Callgraph-based cache analysis [x86 only]

MAQAO
- Assembly instrumentation & optimization [x86 only]

mpiP/mpiPview
- MPI profiling tool and analysis viewer

Open MPI
- Integrated memory checking

Open|Speedshop
- Integrated parallel performance analysis environment

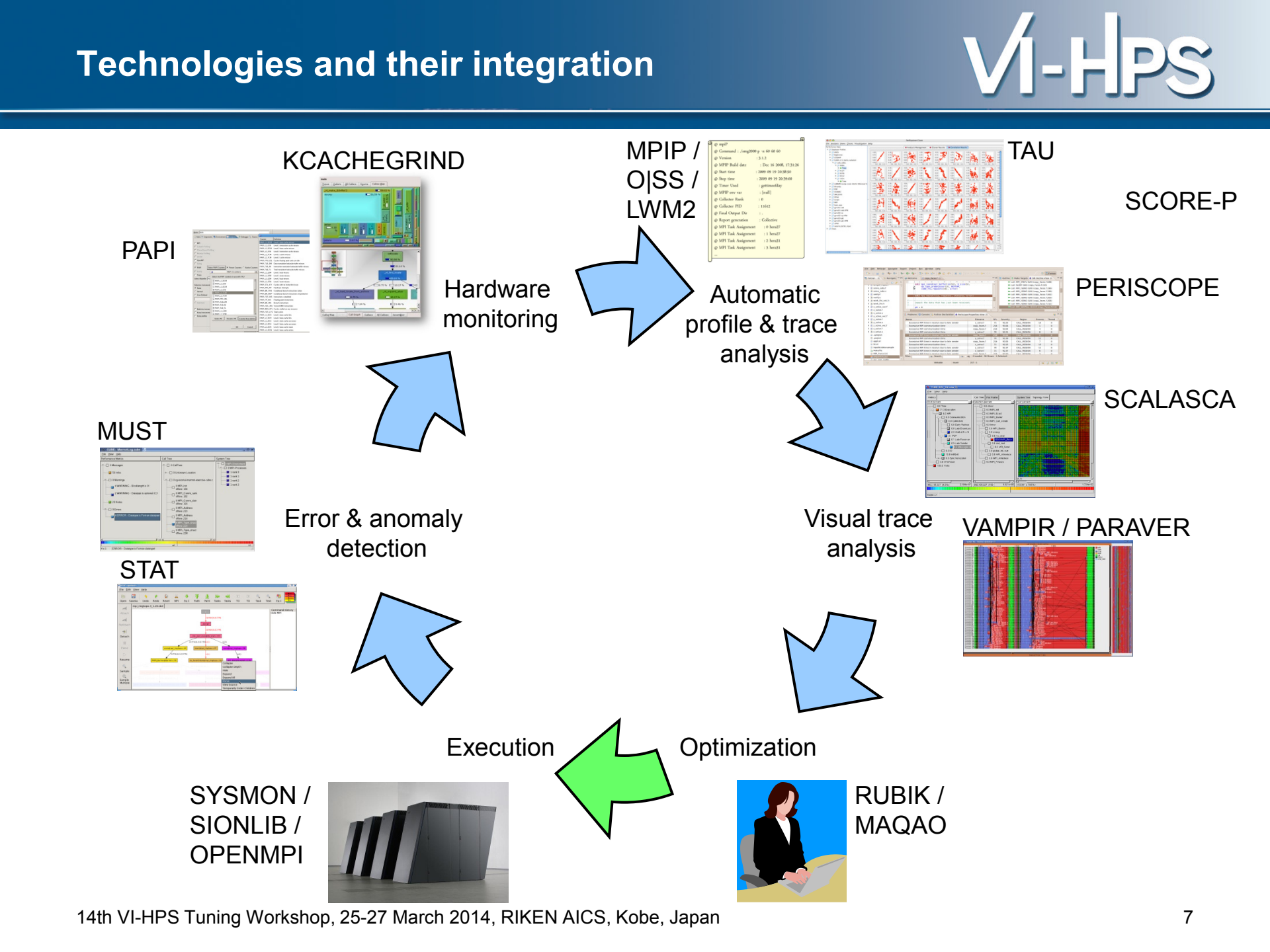
Paraver/Extrae
- Event tracing and graphical trace visualization & analysis

Rubik
- Process mapping generation & optimization [BG only]

SIONlib
- Optimized native parallel file I/O

STAT
- Stack trace analysis tools

Technologies and their integration



Tools will ***not*** automatically make you, your applications or computer systems more *productive*.

However, they can help you understand ***how*** your parallel code executes and ***when / where*** it's necessary to work on *correctness* and *performance* issues.

VI-HPS training & Tuning Workshops

- Goals
  - Give an overview of the programming tools suite
  - Explain the functionality of individual tools
  - Teach how to use the tools effectively
  - Offer hands-on experience and expert assistance using tools
  - Receive feedback from users to guide future development
- For best results, bring & analyze/tune your own code(s)!

- VI-HPS Hands-on Tutorial series
  - SC'08, ICCS'09, SC'09, Cluster'10, SC'10, SC'11, EuroMPI'12, XSEDE'13 (San Diego), SC'13 (Denver)
- VI-HPS Tuning Workshop series
  - 2008 (Aachen & Dresden), 2009 (Jülich & Bremen), 2010 (Garching & Amsterdam/NL), 2011 (Stuttgart & Aachen), 2012 (St-Quentin/F & Garching), 2013 (Saclay/F & Jülich) 2014 (Barcelona/Spain, Kobe/Japan, Saclay/France, Edinburgh/UK)

Upcoming events

- 15th VI-HPS Tuning Workshop (7-10 April, Saclay/F)
  - Hosted by Maison de la Simulation (French PRACE ATC)
  - Score-P, Scalasca, Vampir, TAU, MAQAO
- 16th VI-HPS Tuning Workshop (29.04-01.05, Edinburgh)
  - Hosted by EPCC (UK PATC), using *Archer* Cray XC30
  - Allinea, Score-P, Scalasca, Vampir
- Further events to be determined
  - (one-day) tutorials
    - With guided exercises usually using a Live-ISO
  - (multi-day) training workshops
    - With your own applications on actual HPC systems
- Check www.vi-hps.org/training for announced events
- Contact us if you might be interested in hosting an event

VI-HPS Linux Live DVD/ISO

- Bootable Linux installation on DVD (or USB memory stick)
- Includes everything needed to try out our parallel tools on an 64-bit x86-architecture notebook computer
  - VI-HPS tools: MUST, PAPI, Score-P, Periscope, Scalasca, TAU, Vampir*
  - Also: Eclipse/PTP, TotalView*, etc.
    - * time/capability-limited evaluation licences provided for commercial products
  - GCC (w/ OpenMP), OpenMPI
  - Manuals/User Guides
  - Tutorial exercises & examples
- Produced by U. Oregon PRL
  - Sameer Shende

VI-HPS Linux Live ISO

- ISO image approximately 5GB
  - download latest version from website
  - http://www.vi-hps.org/training/live-iso/
  - optionally create bootable DVD or USB drive
- Boot directly from disk
  - enables hardware counter access and offers best performance, but no save/resume
- Boot within virtual machine (e.g., VirtualBox)
  - faster boot time and can save/resume state, but may not allow hardware counter access
- Boots into Linux environment for HPC
  - supports building and running provided MPI and/or OpenMP parallel application codes
  - and experimentation with VI-HPS (and third-party) tools